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1 Introduction

PI3DPX1203 DP1.3 linear re-driver can be employed in source as well as sink applications. This user manual describes the components and the usage of PI3DPX1203 Demo Board Rev.B. Output swing linearity and gain flatness can be tuned in order to recover input DP signal as desired.

2 Overview

Figure 1 is the block diagram of Pericom PI3DPX1203 demo board and figure 2 shows the top view of the demo board. One DP plug connector (J101) on PI3DPX1203 demo board is used for plugging a source device, such as a DP graphic card. A DP cable can be connected between a DP receptacle connector (J102) on the demo board and a sink device, such as a DP monitor. +5V DC can be employed to the demo board via a mini USB female connector (J103) and/or the source device. Through a 3.3V regulator (U102), PI3DPX1203 on the demo board can then be powered up.

I2C mode is enabled via ON/OFF switch (SW102) if the data stored in the I2C bus is used to program PI3DPX1203. I2C address can be set via ON/OFF switch (SW101) if I2C mode of PI3DPX1203 is selected. Equalization, output linearity and flat gain settings of PI3DPX1203 can be adjusted via the same ON/OFF switches (SW101-2).

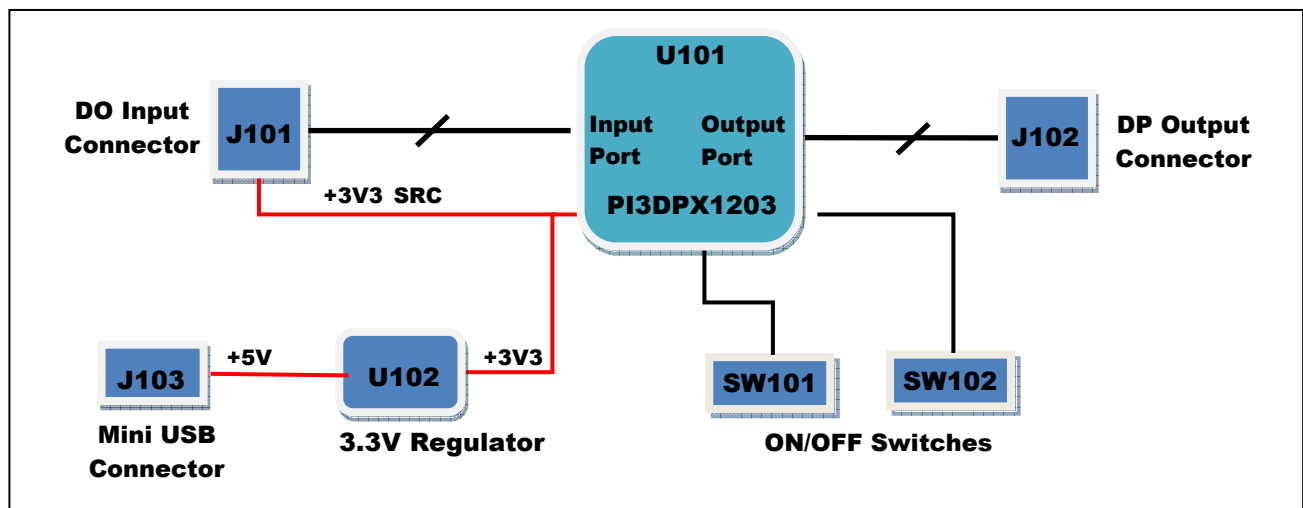


Figure 1: Block Diagram of PI3DPX1203 Demo Board Rev.B

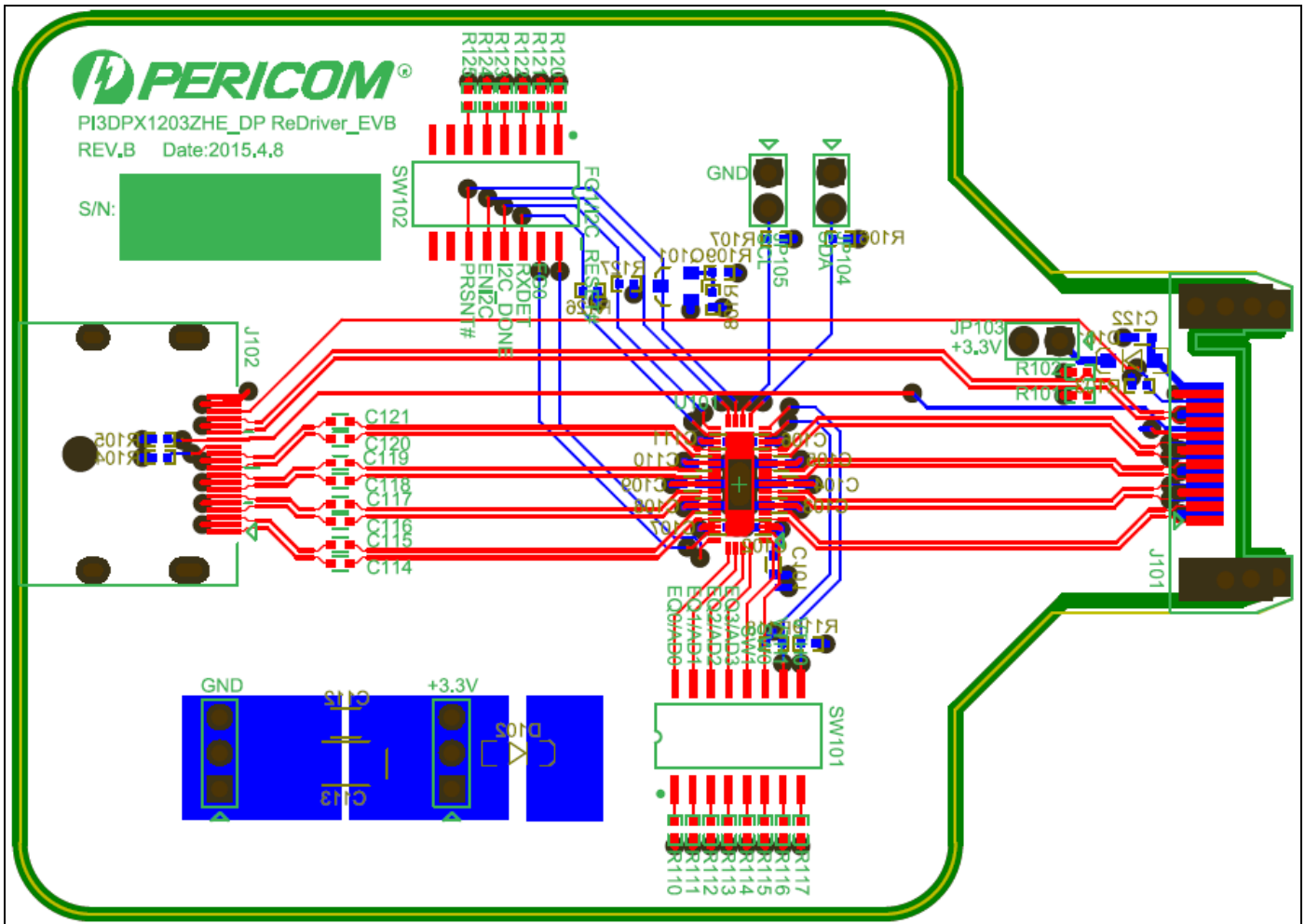


Figure 2: Top View of PI3DPX1203 Demo Board Rev.B

3 Quick Start

To start-up the PI3DPX1203 demo board Rev.B for evaluating PI3DPX1203, complete the following steps:

1. Keep pins 5 and 6 of SW101 switch open so as to set the output linearity of PI3DPX1203 to 1000mV;
2. Leave pin 1 of SW102 switch open while short pins 2 and 15 to set flat gain of PI3DPX1203 to 0dB;
3. Short pins 5 and 12 of SW102 switch so that PI3DPX1203 is programmed to pin control mode;
4. Short pins 1/2/3/4 to 16/15/14/13 of SW101 switch of PI3DPX1203, respectively, to set equalization to 1.8dB;
5. Short JP103 header pin to allow 3.3V from a source device feeding current to PI3DPX1203, or short JP106 header pin and connect a USB adaptor to J103 min USB connector to feed 5V to PI3DPX1203 demo board;
6. Plug J101 DP plug connector to a source device, e.g. graphic card;
7. Connect a sink device, e.g. DP monitor, to J102 DP receptacle connector via a DP cable.

4 Circuit Description

4.1 Equalization Setting

PI3DPX1203 offers several equalization values for covering designs with short and long input PCB traces or cables. The table below provides a reference of EQ settings with various input FR4 trace length and input HDMI cable length.

EQ3	EQ2	EQ1	EQ0	6Gbps Input	Input FR4 Trace (in) or Input DP Cable (m)
0	0	0	0	1.8 dB	2" – 3"
0	0	0	1	2.1 dB	
0	0	1	0	2.5 dB	
0	0	1	1	2.9 dB	
0	1	0	0	3.2 dB	
0	1	0	1	3.6 dB	
0	1	1	0	4.0 dB	
0	1	1	1	4.3 dB	
1	0	0	0	4.7 dB	
1	0	0	1	5.1 dB	2m – 7m
1	0	1	0	5.4 dB	
1	0	1	1	5.8 dB	
1	1	0	0	6.1 dB	
1	1	0	1	6.4 dB	
1	1	1	0	6.7 dB	
1	1	1	1	7.0 dB	

Table 1: EQ Setting of PI3DPX1203 Demo Board Rev.B for Source/Sink Application

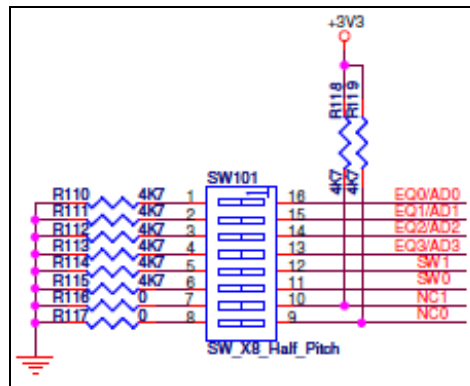


Figure 3: SW101 on PI3DPX1203 Demo Board Rev.B

4.2 Output Linearity Setting

PI3DPX1203 offers four steps of linearity setting in response to the input amplitude changes. Depending on the output trace length, different differential swings may be picked for individual designs. To maintain linearity with respect to the input swing, 1000mV should be chosen.

SW1	SW0	Differential Swing
0	0	700 mV
0	1	800 mV
1	0	900 mV
1	1	1000 mV

Table 2: Output Linearity of PI3DPX1203 Demo Board Rev.B for Source Application

4.3 Flat Gain Setting

The gain of PI3DPX1203 may also need to be tuned with respect to different output trace lengths. For supporting long output cable, maximum flat gain should be set.

FG1	FG0	Gain
0	0	-4 dB
0	1	-2 dB
1	0	0 dB
1	1	2 dB

Table 3: Flat Gain of PI3DPX1203 Demo Board Rev.B

4.4 I2C_MODE/_RESET# Setting

When tying multiple PI3DPX1203 devices to SCL and SDA buses, individual address should be set for each device via AD[3:0] such that its configuration can be loaded from the EEPROM properly. The address of the first device in the sequence must be set to 0x00h. Subsequent devices must follow the address order listed below.

1. U1: AD[3:0] = 0000 = 0x00h
2. U2: AD[3:0] = 0001 = 0x10h
3. U3: AD[3:0] = 0010 = 0x20h
4. U4: AD[3:0] = 0011 = 0x30h

I2C_RESET# and I2C_DONE must be daisy-chained from one device to the next in the following sequence so that EEPROM is read by one device at a time.

1. Tie I2C_DONE of U1 to I2C_RESET# of U2
2. Tie I2C_DONE of U2 to I2C_RESET# of U3
3. Tie I2C_DONE of U3 to I2C_RESET# of U4
4. (Optional) Tie I2C_DONE of U4 to an LED to show the devices have been loaded successfully

4.5 Programming Mode

ENI2C (pin 21) of PI3DPX1203 is used to select between I2C or Pin control mode. It is set via SW102 switch. I2C address at pins 39-42 of PI3DPX1203 is set via SW101 switch. The pins are shared with EQ pins.

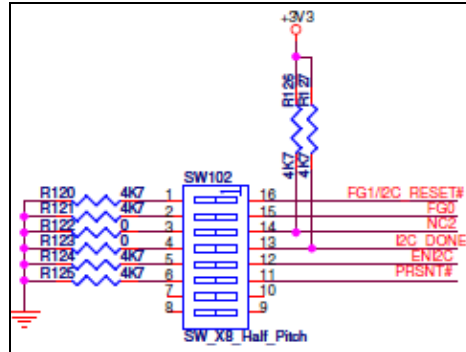


Figure 4: SW102 on PI3DPX1203 Demo Board Rev.B

ENI2C	Pins 5 and 12 of SW102	Programming Mode
L	Short	Pin Control Mode
H	Open	I2C Control Mode

Table 4: ENI2C Setting of PI3DPX1203 Demo Board Rev.B

4.6 5V/3.3V Power Supply

3.3V on PI3DPX1203 demo board rev.B can be fed through three methods.

1. Any source connected to input DP connector J101 via +3V3_SRC power rail providing that JP103 header pin is shorted;
2. Mini-USB adaptor connected to mini USB2.0 connector J103 via +3V3_USB power rail if JP106 header pin is shorted;
3. External power supply via JP101 header pin with JP102 as GND reference.

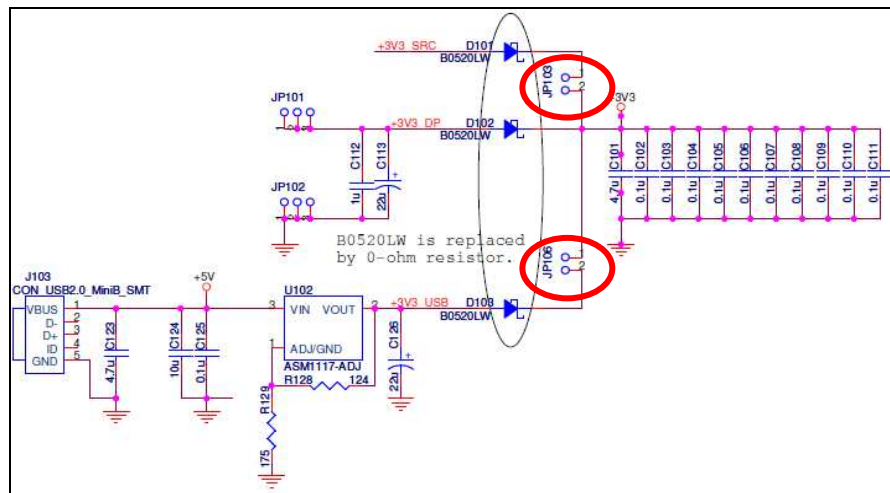


Figure 5: Power Circuit of PI3DPX1203 Demo Board Rev.B

4.7 Power Saving Mode

PI3DPX1203 can enter power saving mode by setting PRSNT# pin to high voltage level. In the schematic, PRSNT# pin is controlled by VCC of PI3DPX1203.

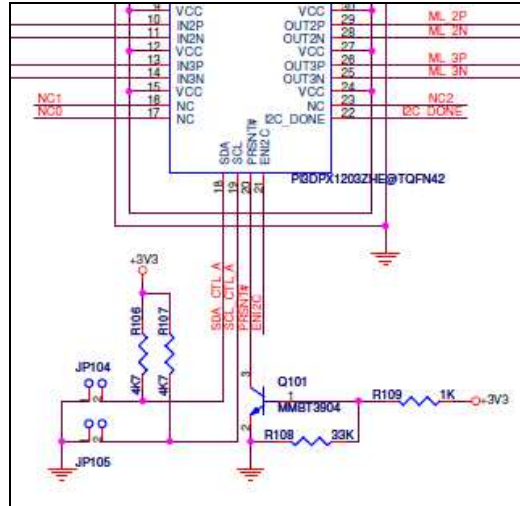


Figure 6: PRSNT# Circuit of PI3DPX1203 Demo Board Rev.B

Alternatively, PRSNT# can be selected via switch SW101.

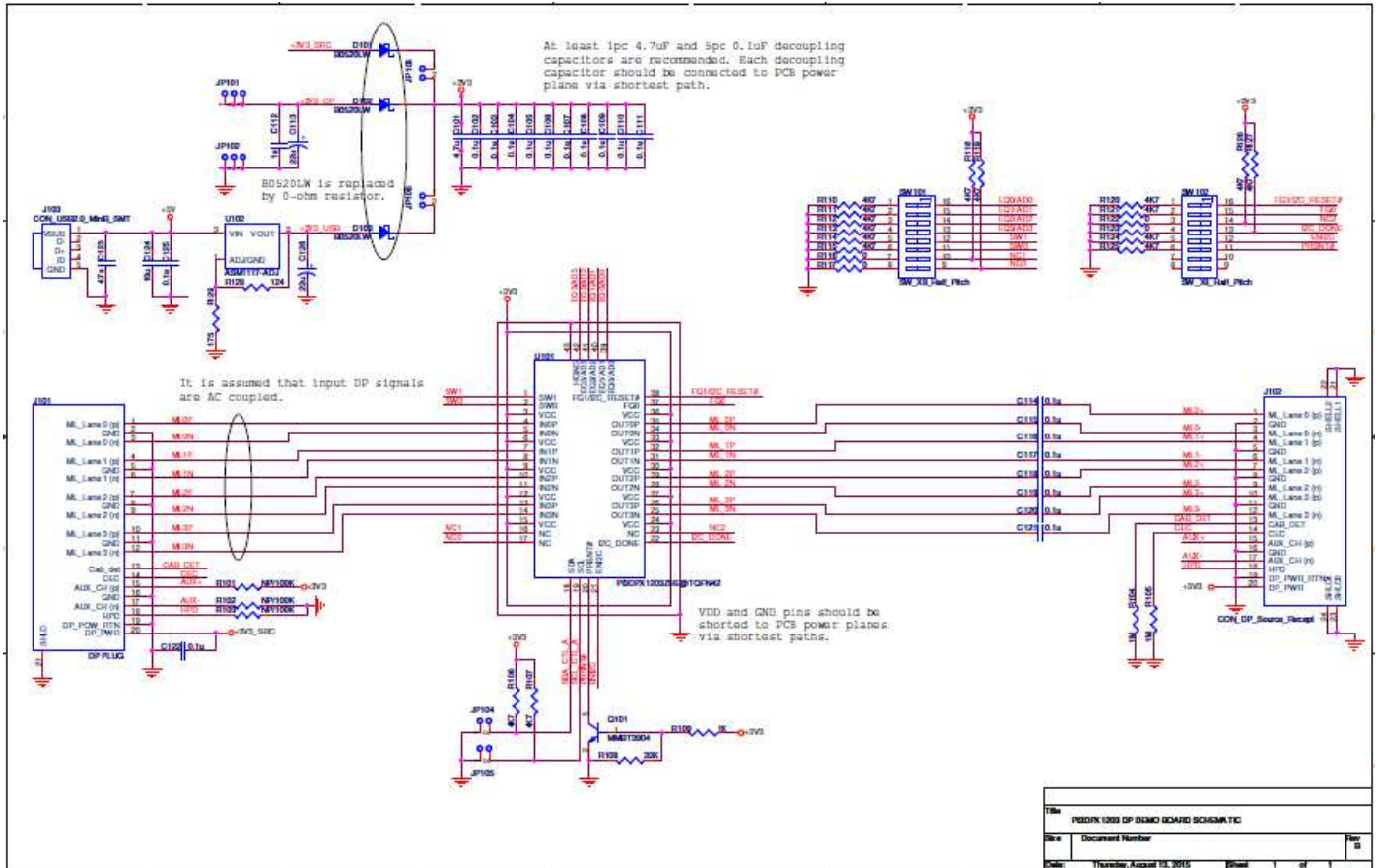
PRSNT#	Pins 6 and 11 of SW102	Output TMD5 of PI3DPX1203
L	Short	Normal Mode
H	Open	Power Saving Mode

Table 5: PRSNT# Setting of PI3DPX1203 Demo Board Rev.B

5 References

- (1) VESA DisplayPort Standard Version 1 Revision 2a, Video Electronics Standards Association, January 5, 2010
- (2) VESA DisplayPort PHY Compliance Test Specification, Version 1.2b, Video Electronics Standards Association, November 26, 2012

6 Appendix A: Demo Board Schematic



For clearer view of schematic diagram, please click the PDF file icon on the right.



P3DPX1203_DP_S
CHEMATIC_REVB_