Application Notes for AP3775 System Solution

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1. Introduction

The AP3775 is an innovative Sub-5mW standby power solution from BCD semiconductor. Combined with the AP4341, the AP3775 power solution can achieve the less 5mW standby power, tight constant voltage regulation and good dynamic performance.

The AP3775 is designed for driving bipolar transistor in Flyback converter, which uses Pulse Frequency Modulation (PFM) method to realize Discontinuous Conduction Mode (DCM) operation for Flyback power supplies.

The AP3775 can provide accurate constant voltage (CV), constant current (CC) regulation with Primary Side Regulation (PSR) structure. It uses internal line compensation and cable compensation to reduce the number of external system components. Fixed cable compensation is used in different IC versions to adapt the different voltage drop on output cable and good CV regulation is achieved. Besides, audio noise is reduced by the creative audio suppression technique.

As to BCD zero Watt standby power solution, there is a secondary controller the AP4341 (IC2) to keep the light load voltage regulation and improve dynamic performance.

The AP3775 solution can apply into 5.0V output voltage Charger/Adapter system which has ultra low standby power requirement.

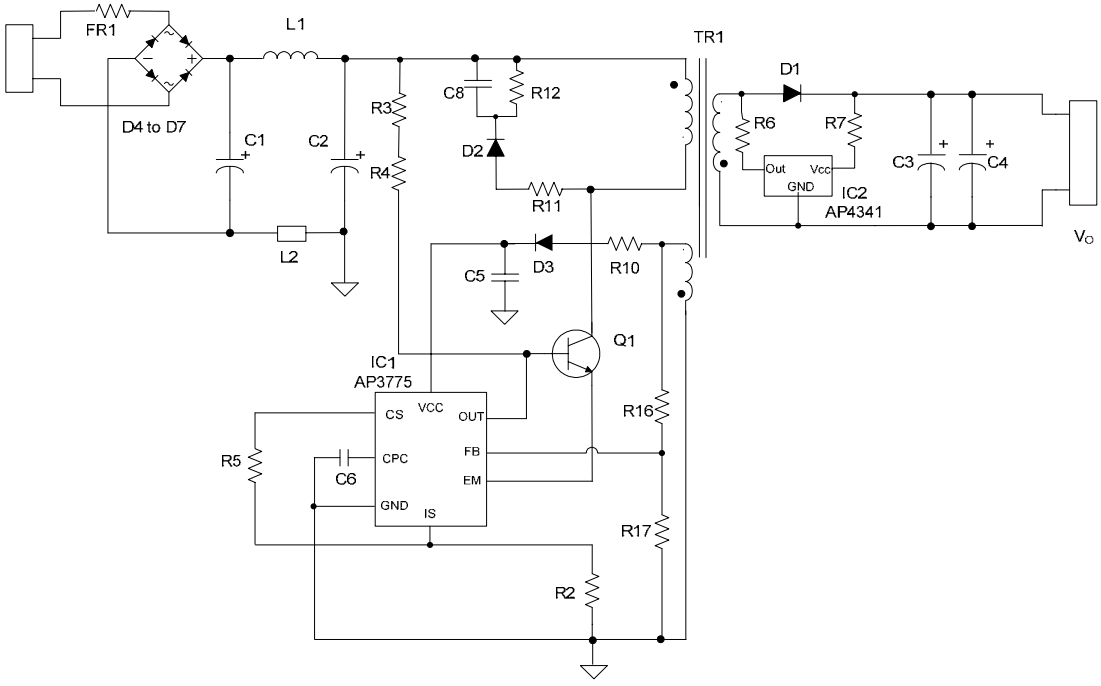

Figure 1. Typical Application Circuit of AP3775

Figure 1 is the typical application circuit of the AP3775, which is a conventional Flyback converter with a 3-winding transformer---primary winding (N_P), secondary winding (N_S) and auxiliary winding (N_A). The auxiliary winding is used for providing V_{CC} supply voltage for IC and sensing the output voltage feedback signal to FB pin.

Figure 2 shows the typical waveforms which demonstrate the basic operating principle of AP3775 application. And the parameters are defined as following.

I_{dri}---The driving signal of primary power switch
I_p---The primary side current
I_s ---The secondary side current
I_{PK}---Peak value of primary side current

I_{PKS}---Peak value of secondary side current
V_{SEC}---The transient voltage at secondary winding
V_S---The stable voltage at secondary winding when rectification diode is in conducting status, which equals the sum of output voltage V_{OUT} and the forward voltage drop of diode
V_{AUX}---The transient voltage at auxiliary winding
V_A---The stable voltage at auxiliary winding when rectification diode is in conducting status, which equals the sum of voltage V_{CC} and the forward voltage drop of auxiliary diode
t_{SW} ---The period of switching frequency
t_{ONP}---The conduction time when primary side switch is "ON"
t_{ONS}---The conduction time when secondary side diode is "ON"
t_{OFF}---The dead time when neither primary side switch nor secondary side diode is "ON"
t_{OFFS}---The time when secondary side diode is "OFF"

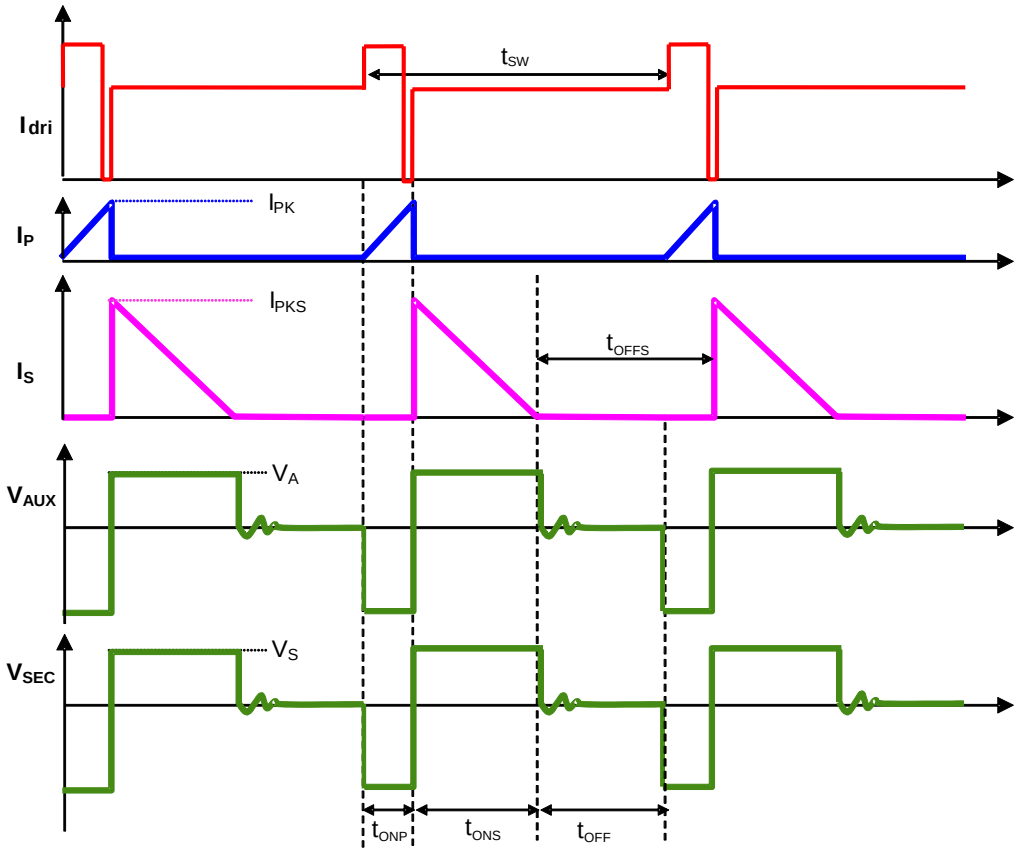

Figure 2. Operation Waveforms of Flyback PSR Control System

LL Mode Operation at Light Load

At no load and light load, the AP3775 works in Low Light mode (LL mode) and the output voltage is detected by AP4341. In order to achieve ultra low standby power, in LL mode, the static current (I_{CC_NL}) of the AP3775 is reduced from 250μA to 100μA, current reference V_{CS} is high to reduce switching frequency.

- The conditions of exiting LL mode---V_{CPC} ≥90mV or t_{OFF}<t_{DELAY}+30μs.
- The conditions of entering LL mode---V_{CPC}<60mV and t_{OFF}≥t_{DELAY}+30μs.

In LL mode, when the AP4341 detects the output voltage is lower than its trigger voltage, the AP4341 OUT pin emits a periodical pulse current. This pulse current will generate a pulse voltage on feedback winding through the transformer coupling. When the AP3775 detects this V_{PULSE} (>100mV is valid), primary switch immediately turns on to provide one energy pulse to supply output terminal and primary V_{CC}.

To achieve low standby power, the lower switching frequency is necessary. But if the off time is too long, the V_{CC} voltage will reduce to very low level. To avoid V_{CC} being lower than UVLO, a minimum switching frequency is specified by the AP4341 (t_{DIS}). If V_O can't be lower than trigger voltage within t_{DIS}, AP4341 OUT pin will emit the periodical pulse current and let the primary switch turn on.

No Load Operation Mode 1

When the transferred energy of one switching pulse can charge the output voltage $V_O \geq V_{DIS}$, the AP4341 will enable a 1mA current to discharge the output voltage, and the power system switching period will be the discharge time of the AP4341. Because the discharge current at no load is very small, the output voltage decreases from V_{DIS} to V_{TRI} very slowly. As the above mentioned, if V_O doesn't decrease to V_{TRI} within T_{DIS}, the primary switch will turn on again. The detailed operation waveform is shown in Figure 3.

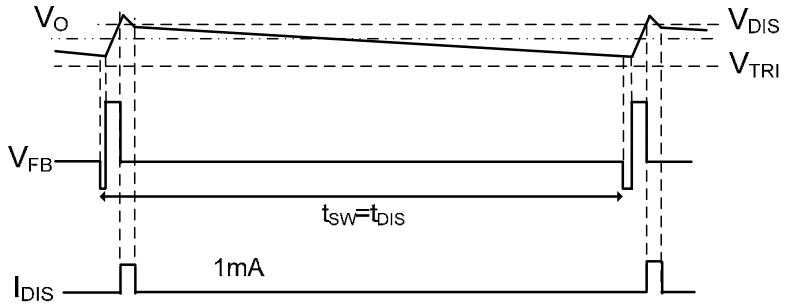

Figure 3. No Load Operation Waveforms Mode 1

No Load Operation Mode 2

When the transferred energy of one switching pulse can't charge the output voltage $V_O \geq V_{DIS}$, then the 1mA discharge current will not be enabled. The output voltage will be discharge to be lower than the trigger voltage of the AP4341 within the discharge time. That means the off time will be smaller than the discharge time t_{DIS} of the AP4341, as shown in Figure 4.

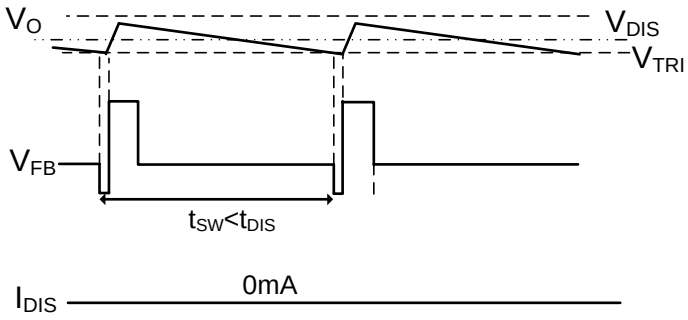

Figure 4. No Load Operation Waveforms Mode 2

Dynamic Response Function_Undershoot

When output load changes from light load to heavy load, the output voltage will decrease. Once the AP4341 detects V_O is lower than V_{TRI}, a pulse current I_{PULSE} will generate. And V_{PULSE} is generated on feedback winding through the transformer coupling due to I_{PULSE}. When the AP3775 detects V_{PULSE} (>90mV is valid), primary switch is "ON". V_{PULSE} will be valid again after a delay time (t_D), which is determined by the AP3775.

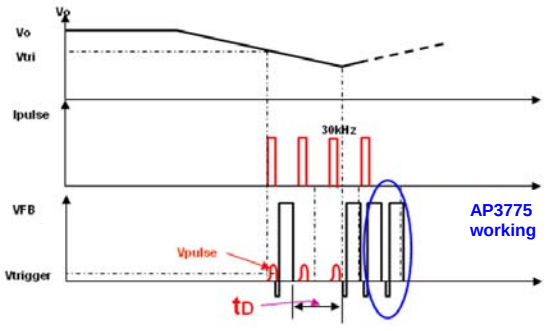

Figure 5. Undershoot Response Waveform

Dynamic Response Function_Overshoot

When output load changes from heavy load to light load, the output voltage will rise. When the AP4341 detects V_O is higher than V_{OVP}, and the off time of the AP3775 (t_{OFF}) is longer than 2ms, a 60mA discharge current will be enabled from VCC pin of the AP4341. Thus the output voltage will fall fast. Once the voltage is lower than V_{OVP}, the 60mA discharge current will stop. Then output voltage falls slowly. When t_{OFF}≥80ms and V_O≥V_{DIS}, 1mA is used to discharge the output voltage.

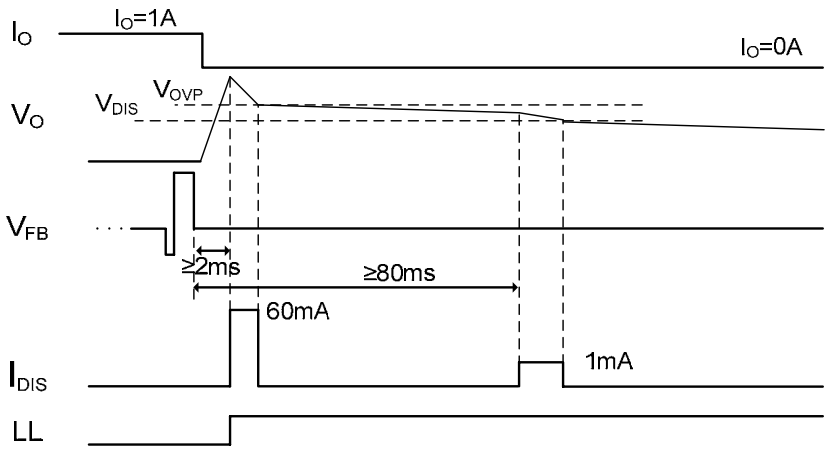

Figure 6. Overshoot Response Waveform

2. Guideline of System Design

1. Low Standby Power Design
2. Switching Frequency Design
3. Transformer and Power Devices Design
4. Feedback Resistors Design
5. Line Compensation Design
6. Cable Compensation Design

2.1 Low Standby Power Design

In order to achieve low standby power, the AP3775 decreases the minimum operating frequency and operating current I_{CC_NL}. The power loss of the AP3775 is,

$$P_{U1} = V_{CC} \times I_{CC\_NL} \quad (1)$$

Generally, the resistor startup circuit takes the considerable power loss at no load condition since of the lower startup resistance to guarantee the shorter startup time. The AP3775 solution uses the innovative zero power dissipation startup circuit. The AP3775 uses BJT Q1's current amplifying function, which the startup current will be amplified to over ten times, so that the startup resistors R3+R4 value can be increased to high enough. The loss of startup resistors is,

$$P_{START} = \left(V_{indc\_nor} - V_{TH\_ST}\right)^2 / (R3 + R4) \quad (2)$$

Where V_{TH_ST} is the Startup Threshold of V_{CC}, V_{indc_nor} is the rectified DC voltage from the nominal AC input voltage.

The AP4341 (IC2) is used to detect the output voltage and decide the no load operating frequency. Thus, the output voltage regulation will keep within ±5% at the whole of line and load condition. The power loss of this secondary controller is,

$$P_{U2} = V_o \times I_{IC2} \quad (3)$$

Where V_O is output voltage and is used as the supplier of the AP4341; I_{IC2} is operating current of the AP4341.

2.2 Switching Frequency Design

As we know, in DCM Flyback converter, the stored energy of primary side will be transferred to secondary side at the time when the primary switch is turned off. And assume the current transfer efficiency from primary to secondary is η_i, then

$$Ipks = Ipk \cdot N_{PS} \cdot \eta_i \quad (4)$$

Here, N_{PS} is the turn ratio of primary winding to secondary winding.

It is obvious that the output current I_O is the average current of secondary side I_S,

$$Io = \frac{1}{2} Ipks \cdot \frac{t_{ONS}}{t_{SW}} \quad (5)$$

Then,

$$Io = \frac{1}{2} Ipk \cdot N_{PS} \cdot \eta_i \cdot \frac{t_{ONS}}{t_{SW}} \quad (6)$$

Always voltage of CPC pin (V_{CPC}) is determined by,

$$Vcpc = V_{DD} \cdot \frac{t_{ONS}}{t_{SW}} \quad (7)$$

Here V_{DD} is a constant voltage generated by IC. Then,

$$\frac{Vcpc}{I_O} = \frac{2 \cdot V_{DD}}{N_{PS} \cdot \eta_i \cdot I_{PK}} \quad (8)$$

If η_T is efficiency of power transmission from transformer primary to the output, then

$$P_O = V_O \cdot I_O = \frac{1}{2} \cdot L_P \cdot I_{pk}^{\ 2} \cdot f_{SW} \cdot \eta_T \quad (9)$$

Where, f_{SW} is the switching frequency. So,

$$\frac{f_{SW}}{I_O} = \frac{2 \cdot V_O}{L_P \cdot I_{pk}^{\ 2} \cdot \eta_T} \quad (10)$$

When voltage at the sense resistor reaches the reference voltage set by the AP3775, the switch will be turned off and primary current reaches its maximum value,

$$I_{PK} = \frac{V_{cs\_ref}}{R_{cs}} \quad (11)$$

When the constant reference V_{CS_REF} is used, the peak current I_{PK} is constant. From formula (8) and (10), it is obvious that V_{CPC} and f_{SW} increase linearly with the output current I_O.

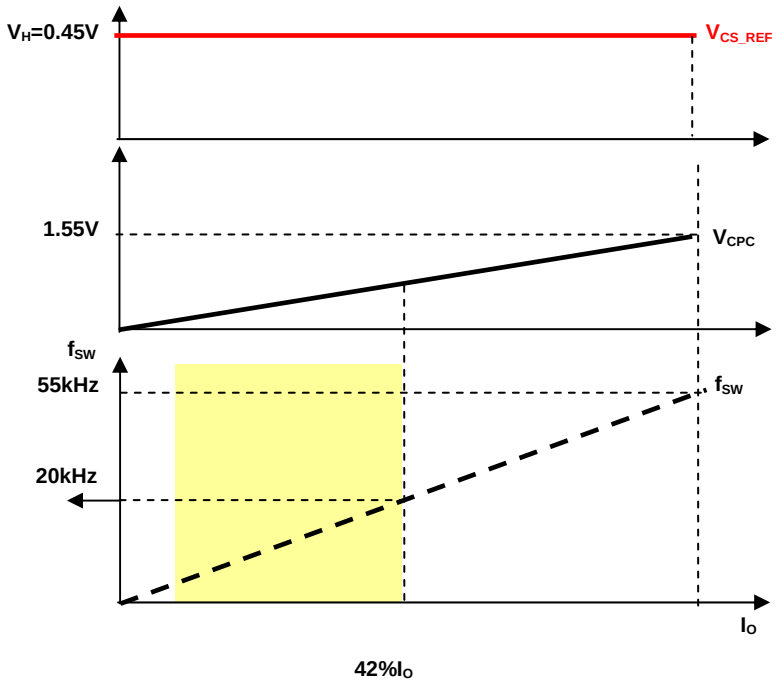

Figure 7. Relationship between V_{CPC}, f_{SW} and I_O at Constant Peak Current Mode

In the AP3775, in order to realize audio noise suppression, two-segmented of current reference voltage V_{CS_REF} is used except LL mode. The reference is about 0.45V when I_O>=42%*I_{O_MAX} and is decreased to 0.45V/1.5 when I_O<42%* I_{O_MAX}, as follows in Figure 8.

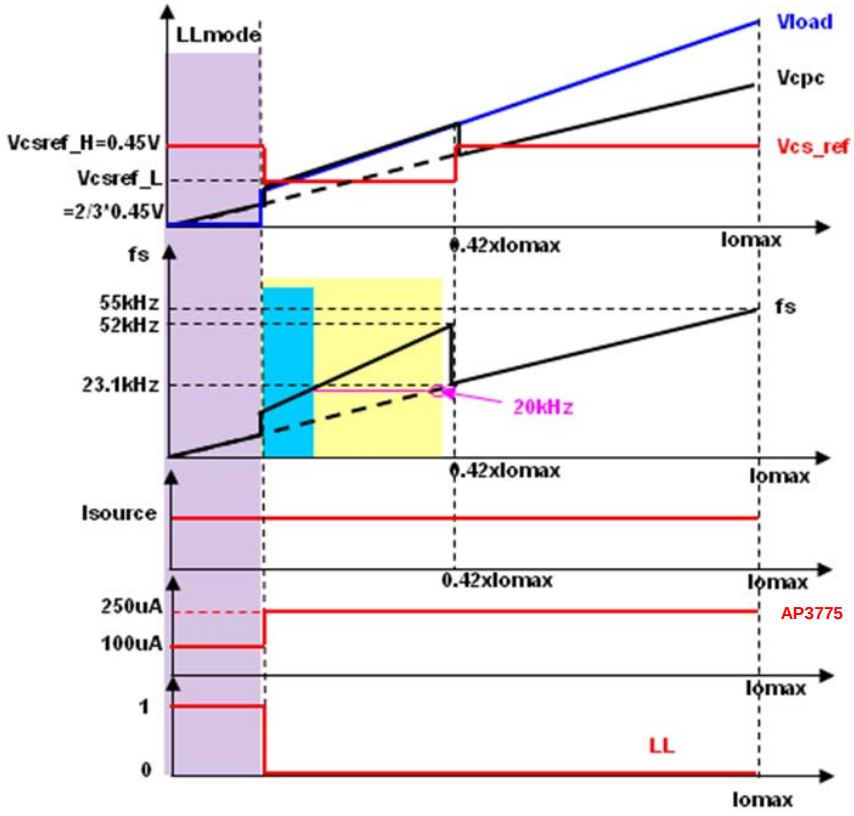

Figure 8. Relationship between V_{CPC}, f_{SW} and I_O at Variable Peak Current Mode

Then from formula (8) and (10), we can see the V_{CPC} and f_{SW} both has a leap at about 42% of maximum load. At the leap point, if the peak current is decreased by 1.5 times, the voltage of CPC pin at low I_{PK} will be increased to 1.5 times, and the switching frequency f_{SW} at low I_{PK} will be increased to 1.5^2 times. So the load range in audio is largely narrowed.

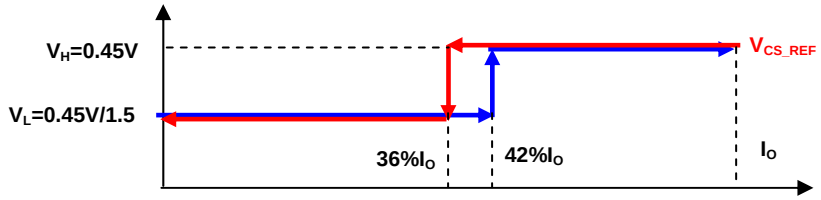

Figure 9. Hysteresis at Conversion between Low I_{PK} and High I_{PK}

In order to avoid unstable operation, a hysteresis is added at the conversion between low I_{PK} and high I_{PK}. Considering the relationship between audio noise and flux density of transformer, deltaB≤2500 gauss is better for audio noise suppression.

The low limitation of maximum switching frequency is given by audio noise suppression. And the upper limit of the AP3775 can be up to 120kHz. But this is only the limit of the IC; the finally designed maximum switching frequency is determined by the tradeoff between the efficiency, mechanical dimensions and thermal performance.

2.3 Transformer and Power Devices Design

In the design of AP3775, constant current control function will keep a fixed proportion between on-time t_{ONS} and off-time t_{OFFS} of rectifier D1 (in Figure 1) by discharging or charging a capacitor embedded in the IC. The fixed proportion is,

$$\frac{t_{ONS}}{t_{SW}} = \frac{4}{9} \tag{12}$$

It is assumed,

$$k = \frac{2 \cdot t_{SW}}{t_{ONS}} = 4.5 \tag{13}$$

Then the output constant-current value I_O is,

$$I_O = \frac{1}{k} \cdot I_{PKS} = \frac{1}{k} \cdot N_{PS} \cdot \eta_i \cdot I_{PK} \tag{14}$$

2.3.1 Calculate Turn Ratio of Transformer (N_{PS})

The turn ratio of transformer should be designed first, which ensures the power converter operating in DCM within the whole conditions,

$$t_{SW} \geq t_{ONP} + t_{ONS} \tag{15}$$

As we know, if equation (13) is met at minimum input voltage and full load, it can ensure that the power converter operates in DCM in all conditions.

For the primary side current,

$$t_{ONP} = I_{pk} \cdot \frac{L_p}{V_{indc}} \tag{16}$$

Where LP is the inductance of primary winding.

V_{indc} is the rectified DC voltage of input.

When V_{indc} is the minimum value, the maximum t_{ONP} can be obtained. So,

$$t_{ONP\_MAX} = I_{pk} \cdot \frac{L_p}{V_{indc\_min}} \tag{17}$$

For the secondary side current, L_S is the inductance of secondary winding, V_d is the forward voltage of secondary diode.

There is an oscillating signal on FB waveform after secondary Schottky diode current decrease to zero, which is caused by primary inductance and equivalent output capacitance of primary switch. Then some margin is added to t_{ons} as,

$$t_{ONS} = I_{pks} \cdot \frac{L_S}{V_S} \cdot 1.1 \tag{18}$$

$$V_S = V_O + V_d \tag{19}$$

From formula (4) and formula (14), we can get,

$$Vs \cdot Io = \frac{1}{2} \cdot Ls \cdot Ipks^2 \cdot fsw = \frac{1}{2} \cdot \frac{Lp}{N_{PS}^2} \cdot (Ipk \cdot N_{PS} \cdot \eta i)^2 \cdot fsw$$
$$= \frac{1}{2} \cdot Lp \cdot Ipk^2 \cdot fsw \cdot \eta i^2 \tag{20}$$

Then,

$$t_{SW} = \frac{L_p \cdot I_{pk}^2 \cdot \eta_i^2}{2 \cdot V_S \cdot I_O} \tag{21}$$

t_{ONP}, t_{ONS} and t_{SW} in (15) are replaced with (16), (18) and (21), then

$$\frac{L_p \cdot I_{pk}^2 \cdot \eta_i^2}{2 \cdot V_S \cdot I_O} \geq I_{pks} \cdot \frac{L_s}{V_s} \cdot 1.1 + I_{pk} \cdot \frac{L_p}{V_{indc\_min}} \tag{22}$$

Relationship between inductance of primary side and secondary side is,

$$L_s = \frac{L_p}{N_{PS}^2} \tag{23}$$

At full load, the system will work in the boundary of CC regulation. I_O can be given by formula (14)，the following can be obtained,

$$N_{PS} \leq N_{PS\_MAX} = \frac{V_{indc\_min} \cdot \eta_i}{V_S} \cdot \left(\frac{k}{2} - 1.1 \right) \tag{24}$$

Then designed turns ratio N_{PS} should be no more than N_{PS_MAX} defined in formula (24).

2.3.2 Check stress voltage of primary side switch and reverse voltage of secondary diode

If N_{PS} is fixed by customer according in design step 2.3.1, real stress voltage of primary side switch and reverse voltage of secondary diode can be calculated.

The maximum stress voltage of primary side switch is,

$$V_{ds\_switch} = V_{dc\_spike} + V_{indc\_max} + \frac{V_S \cdot N_P}{N_S} \quad (25)$$

Be careful that the value of V_{dc_spike} is determined by the snubber circuit design.

Maximum reverse voltage of secondary side,

$$V_{dr} = V_S + \frac{V_{indc\_max} \cdot N_S}{N_P} \quad (26)$$

For Flyback converter design, higher turns ratio N_{PS} brings higher stress voltage of primary side switch, higher transforming efficiency, and the lower reverse voltage of secondary diode. Finally, in design of turns ratio N_{PS} and N_{PA}, formula (24), (25), (26), should be totally considered.

2.3.3 Calculate the peak current of primary side and current sensed resistor (I_{PK} & R_{CS})

I_{PK} can be calculated by the output current.

$$I_{pk} = \frac{k \cdot I_O}{N_{PS} \cdot \eta_i} \quad (27)$$

In the AP3775, 0.45V is an internal reference voltage. If the sensed voltage V_{CS_REF} reaches 0.45V, the power switch will shut down and t_{ONP} will be ended.

$$R_{CS} = \frac{V_{cs\_ref}}{I_{pk}} \quad (28)$$

So R_{CS} can be obtained and selected with a real value from the standard resistor series. We recommended using 1% tolerance resistors for R_{CS}. After R_{CS} is selected, I_{PK} should be modified based on the selected R_{CS}.

2.3.4 Calculate the inductance of primary side---L_P

The primary side inductance L_P is relative with the stored energy. L_P should be big enough to store enough energy, so that P_{O_MAX} can be obtained from this system.

According to formula (20), the output power can be given by,

$$P_S = V_S \cdot I_O = \frac{1}{2} \cdot L_p \cdot I_{pk}^2 \cdot f_{SW} \cdot \eta_i^2 \quad (29)$$

Where, f_{SW} was set by the user based on definite requirement. Then, L_P can be gotten by,

$$L_P = \frac{2 \cdot P_S}{I_{PK}^2 \cdot f_{SW}} \cdot \frac{1}{\eta_i^2} \quad (30)$$

2.3.5 Calculate the turns of primary, secondary and auxiliary (N_P, N_S, N_A)

The turns of primary winding,

$$N_p = \frac{L_P \cdot I_{PK}}{Ae \cdot \Delta B} \geq \frac{L_P \cdot I_{PK}}{Ae \cdot B\max} \quad (31)$$

As N_{PS} and N_P are fixed, we can get N_S by,

$$N_S = \frac{N_P}{N_{PS}} \quad (32)$$

Turns of auxiliary winding is,

$$N_A = \frac{N_S \cdot V_A}{V_S} \quad (33)$$

2.3.6 Check the maximum duty cycle of primary side

After turn ratio of primary side and secondary side is designed, the maximum duty cycle of primary side at low line voltage can be calculated again.

Considering the Volt-second balance between magnetizing and de-magnetizing, the formula of duty cycle is,

$$D_{\max} = \frac{(V_O + V_d) \cdot N}{V_{indc} \cdot \eta_i} \cdot \frac{t_{ons}}{t_{sw}} \quad (34)$$

2.3.7 Check reverse voltage of auxiliary diode

If N_P and N_A are fixed according in design step 2.3.5, real reverse voltage of auxiliary diode can be calculated by formulas (26).

2.4 Feedback Resistors Design

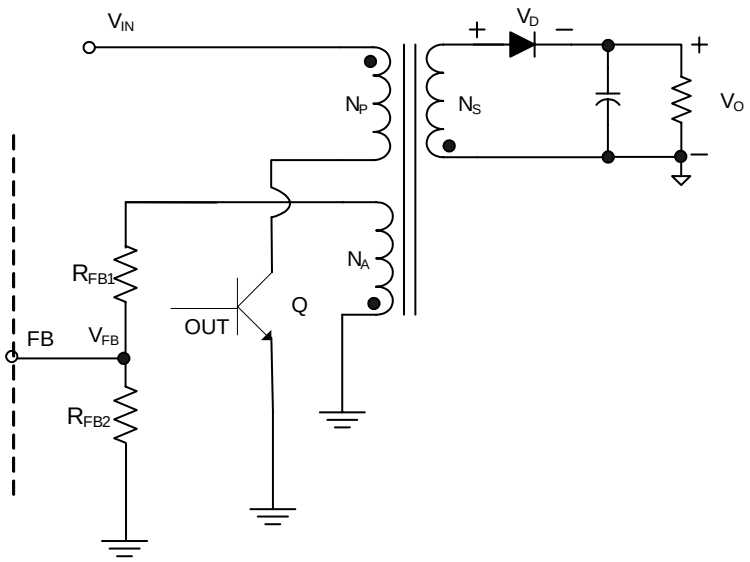

Figure 10. Feedback Resistors Circuit

From above Figure 10,

$$V_o = V_{FB} \cdot \frac{(R_{FB1} + R_{FB2})}{R_{FB2}} \cdot \frac{N_S}{N_A} - V_D \quad (35)$$

$$\frac{R_{FB1}}{R_{FB2}} = \frac{V_o + V_D}{N_S \cdot V_{FB}} \cdot N_A - 1 \quad (36)$$

Through adjusting R_{FB1} and R_{FB2}, a suitable output voltage can be achieved. The recommended values of R_{FB1} and R_{FB2} are within 5kΩ to 100kΩ.

2.5 Line Compensation Design

The internal line compensation function in the AP3775 is shown in Figure 11. S1 is closed when the primary switch is "ON". The line voltage can be detected from the FB pin. The detected voltage internally compensates the peak current. So the line compensation is determined by R_{LINE}. In different applications, the value of R_{LINE} is different.

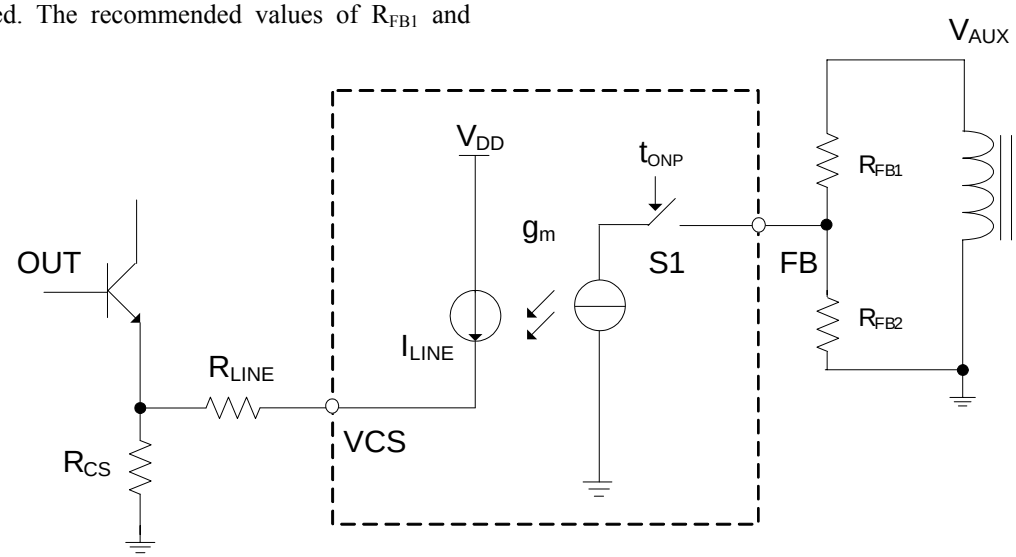

Figure 11. Line Compensation Circuit

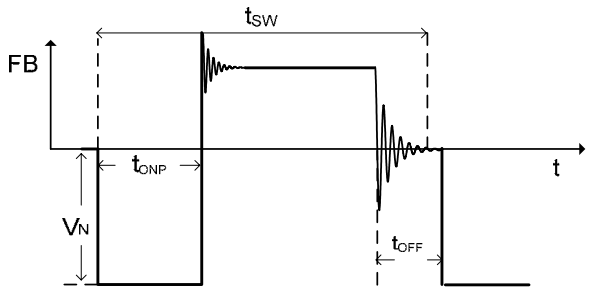

Figure 12. Waveform of FB Pin

The negative voltage V_N of FB pin (in Figure12) is linear to line voltage. The AP3775 samples V_N to realize the line compensation.

$$V_N = V_{indc} \cdot \frac{N_A}{N_P} \cdot \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \quad (37)$$

The compensated voltage of line compensation (V_{CS_LINE}) can be calculated by the following formula,

$$V_{CS\_LINE} = V_{in\_DC} \cdot \frac{N_A}{N_P} \cdot \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \cdot g_m \cdot R_{LINE} \quad (38)$$

This is designed to compensate the additional voltage of V_{CS} introduced by t_{delay}, which is the delay time of internal drivers of IC and primary side switch.

$$V_{delta} = V_{indc} \cdot \frac{t_{delay}}{L_P} \cdot R_{cs} \quad (39)$$

Then R_{LINE} can be adjusted to achieve excellent line regulation of output current.

$$R_{LINE} = (\frac{t_{delay}}{Lp} \cdot R_{cs}) / (\frac{N_A}{N_P} \cdot \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \cdot g_m) \quad (40)$$

2.6 Cable Compensation Design

Two versions of IC are designed to meet different requirement for cable voltage compensation. As we know, an increase voltage at V_{FB} (ΔV_{FB_CABLE}) will introduce an increase voltage at V_{OUT} (ΔV_{OUT_CABLE}), which is a linear function of the output load (I_{OUT}). Then in application of the AP3775, CPC pin detects the load information and a corresponding delta voltage is added to V_{FB} to compensate the voltage drop at output cable.

As defined in datasheet below, for example, in the AP3775, there is a total voltage increase of 6% at V_{FB} when the output is at full load (I_{OUT_MAX}). And if the output is at 10%*I_{OUT_MAX}, the increase voltage of V_{FB} is 0.6%. Proper version of IC can be chosen according to the resistance of the output cable.

CABLE COMPENSATION SECTION						
Cable Compensation Voltage	V_{FB_CABLE}/V_{FB} %	AP3775	5	6	7	%
		AP3775B	3	4	5	%

Assume,

$$\Delta V_{FB}\% = \frac{\Delta V_{FB\_CABLE}}{V_{FB}} \quad (41)$$

Then from Figure 8,

$$\Delta V_{OUT\_CABLE} = \Delta V_{FB}\% \cdot V_{FB} \cdot \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \cdot \frac{N_S}{N_A} = I_{O\_MAX} \cdot R_{CABLE} \quad (42)$$

Then after ΔV_{FB}% is calculated, proper version of the AP3775 can be chosen accordingly.

$$\Delta V_{FB}\% = I_{O\_MAX} \cdot R_{CABLE} / (V_{FB} \cdot \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \cdot \frac{N_S}{N_A}) \quad (43)$$

Design Example (for 5V/1.2A application):

Specification:
Input voltage: $85V_{AC}$ to $265V_{AC}$
Output voltage @ cable: V_{O_CABLE}=5V
Output current: I_O=1.2A
Output voltage @ PCB: V_O=5.13V, (AWG26 Cable, Length of Cable=100cm, R_{CABLE}=0.267Ω)

Other setting by users:
Switching frequency: f_{SW}=65kHz
Forward voltage of secondary diode: V_d=0.4V
Forward voltage of auxiliary diode: V_{da}=1.1V
V_{CC} voltage: V_{CC}=14V
Core_type: RM5 (Ae=23.7mm^2), B_{MAX}<3000GS
V_{dc_spike}=50V (with snubber circuit)

Design Steps:

1) Calculate Turn Ratio of Transformer (N_{PS})

$$N_{PS} \le N_{PS\_MAX} = \frac{V_{indc\_min} \cdot \eta_i}{V_S} \cdot \left(\frac{k}{2} - 1.1\right) = 15.8 \quad (44)$$

$$V_{indc\_min} = V_{inac\_min} \cdot \sqrt{2} - 40 \quad (45)$$

Considering some margin for Flyback PSR control, we choose N_{PS}=15.

2) Check stress voltage of primary side switch and reverse voltage of secondary diode.

According to formulas (25), (26) and the selected N_{PS}, proper power devices could be chosen.

$$V_{ds\_switch} = V_{dc\_spike} + V_{indc\_max} + \frac{V_S \cdot N_P}{N_S} = 505V < 700V \quad (46)$$

$$V_{dr} = V_S + \frac{V_{indc\_max} \cdot N_S}{N_P} = 30V < 40V \quad (47)$$

3) Calculate the peak current of primary side and current sense resistor (I_{PK} & R_{CS})

$$I_{pk} = \frac{I_{pks}}{N \cdot \eta_i} = \frac{k \cdot I_O}{N \cdot \eta_i} \approx 380mA \quad (48)$$

$$R_{CS} = \frac{V_{CS}}{I_{pk}} \approx 1.2\,\Omega \quad (49)$$

4) Calculate the inductance of primary side---L_P

$$L_P = \frac{2 \cdot V_S \cdot I_O}{I_{PK}^2 \cdot f_{SW} \cdot \eta_i^2} = 1.5mH \quad (50)$$

5) Calculate the turns of primary, secondary and auxiliary (N_P, N_S, N_A)

$$N_p = \frac{L_P \cdot I_{PK}}{Ae \cdot \Delta B} \ge \frac{L_P \cdot I_{PK}}{Ae \cdot B\max} = 65\,T \quad (51)$$

We choose N_P=90T

$$N_S = \frac{N_P}{N} = 6\,T \quad (52)$$

$$N_A = \frac{N_S \cdot V_A}{V_S} = 16\,T \quad (53)$$

6) Check the maximum duty cycle of primary side

The maximum duty cycle of primary side is calculated as following,

$$D = \frac{(V_O + V_d) \cdot N \cdot 0.4}{V_{indc} \cdot \eta_i} = 0.43 \quad (54)$$

7) Check reverse voltage of auxiliary diode

$$V_{dar} = V_A + \frac{V_{indc\_max} \cdot N_A}{N_P} = 80V \quad (55)$$

8) Feedback Resistors

$$\frac{R_{FB1}}{R_{FB2}} = \frac{V_o + V_D}{N_S \cdot V_{FB}} \cdot N_A - 1 = 2.98 \quad (56)$$

R_{FB1}=29.8kΩ, R_{FB2}=10kΩ

9) Line Compensation Resistors

$$R_{LINE} = \left(\frac{t_{delay}}{Lp} \cdot R_{cs}\right) / \left(\frac{N_A}{N_P} \cdot \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \cdot g_m\right) = 6.3k\,\Omega \quad (57)$$

10) Cable Compensation Choice

V_{FB}=3.7V, the same in two versions of the AP3775. Then,

$$V_{FB}\% = I_{O\_MAX} \cdot R_{CABLE} / \left(V_{FB} \cdot \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \cdot \frac{N_S}{N_A}\right) = 5.8\% \quad (58)$$

According to datasheet information, the AP3775 is a better choice.

$$V_{O\_FL} = V_{O\_NL} + \left(V_{FB}\% \cdot V_{FB} \cdot \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \cdot \frac{N_S}{N_A}\right) - I_{O\_MAX} \cdot R_{CABLE} = 5.01V \quad (59)$$

Where V_{O_NL}=5V. Therefore, the output voltage at cable terminal at full load is a little higher than the voltage at light load.

Design Results Summary

1.Maximum peak current of primary side and R_{CS}			
I_{PK}	380	mA	Peak current of primary side
R_{CS}	1.2	Ω	Current sensed resistor
2.Transformer			
L_P	1.5	mH	Inductance of primary side
N_{PS}	15		Turn ratio of primary and secondary
N_P	90	T	Turns of primary side
N_S	6	T	Turns of secondary side
N_A	16	T	Turns of auxiliary side
D_{MAX}	0.43		Maximum duty cycle of primary side at V_{INDC}=80V
3. Primary power switch and diode			
V_{ds_switch}	505	V	Voltage stress of primary power switch
V_{dr}	30	V	Maximum reverse voltage of secondary diode
V_{dar}	80	V	Maximum reverse voltage of auxiliary diode
4. Voltage feedback resistors			
R_{FB1}	28.9k	Ω	Feedback resistor at upside from auxiliary side to FB pin
R_{FB2}	10k	Ω	Feedback resistor at downside from FB pin to GND
5. Line compensation resistor			
R_{LINE}	6.3k	Ω	Line compensation resistor
6.Cable Compensation			
IC version	AP3775		
V_{O_NL}	5	V	Output voltage @ light load
V_{O_FL}	5.01	V	Output voltage @ full load

3. Summary

In order to get good performance of the AP3775, it is important to correctly design standby power, switching frequency, transformer parameters, feedback resistance and line compensation resistance. This application note only gives a preliminary design guideline about these aspects and considers ideal conditions, so some parameters need to be adjusted slightly on the basis of the calculated results.

4. Application of AP3775 with AP4341

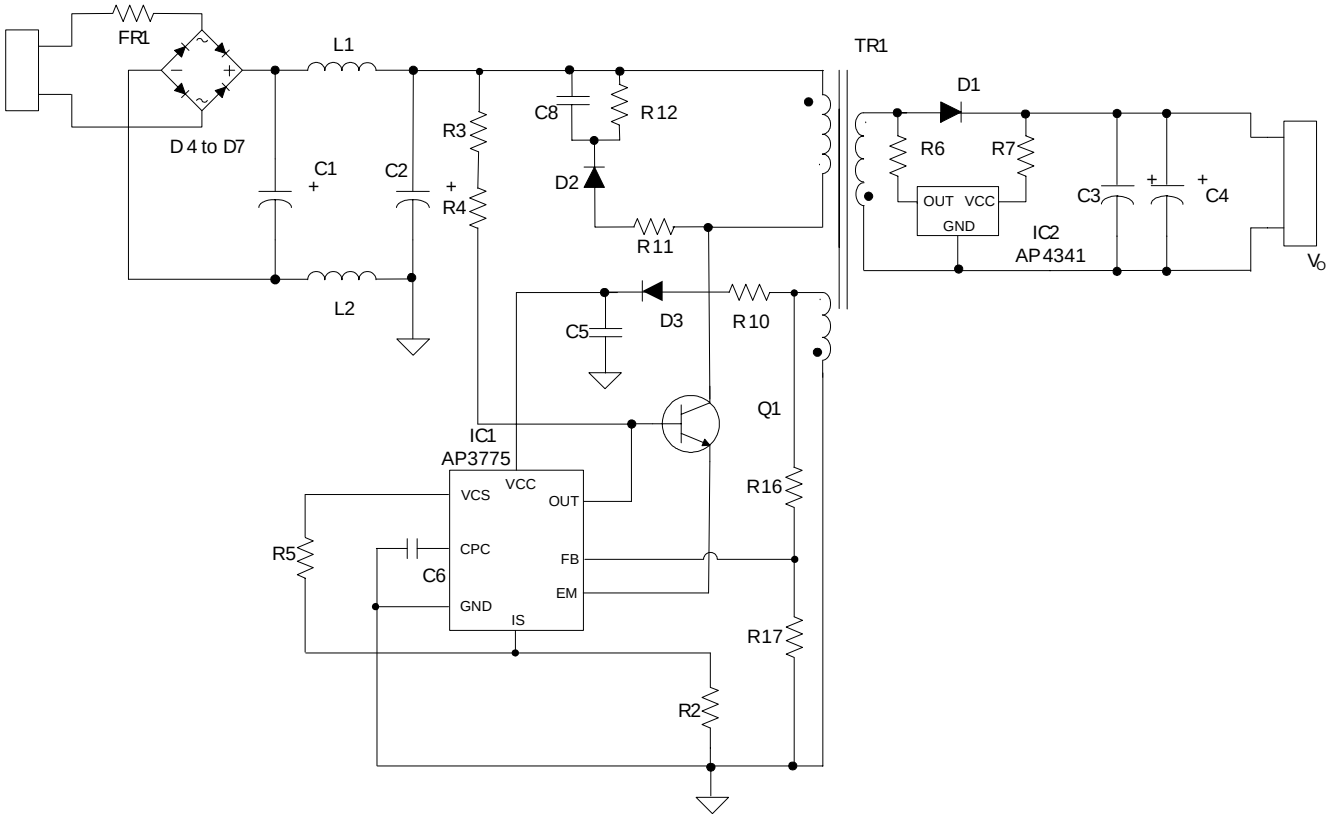

Figure 13. Typical Application Circuit of AP3775 with AP4341

In Primary Side Regulation of the AP3775 application, the AP4341 must be used at secondary side as the output voltage regulator at light load, excellent dynamic response and low standby power can be achieved. When detecting the output voltage lower than a certain level, AP4341 outputs periodical signals which will be coupled to auxiliary side and detected by the AP3775, and the AP3775 will begin an operating pulse, then the output voltage will rise. By fast response and cooperation, the AP4341 and AP3775 can maintain a constant output voltage with very low operating frequency at light load and also can effectively improve the transient performance for Primary Side Regulation power system. Beside, dummy load is not needed at secondary side and as a result standby power will be decreased.