Application Notes for AP4340/L System Solution

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1. Introduction

The AP4340/L is an output voltage detector for Primary Side Regulation (PSR) System. It provides a periodical signal when detecting the output voltage is lower than certain level. The periodical signal can be coupled by the transformer to the primary side, and provided as a triggering primary switch turn on signal for the main controller. By fast response to secondary side voltage, the AP4340/L can effectively improve the transient performance for PSR system.

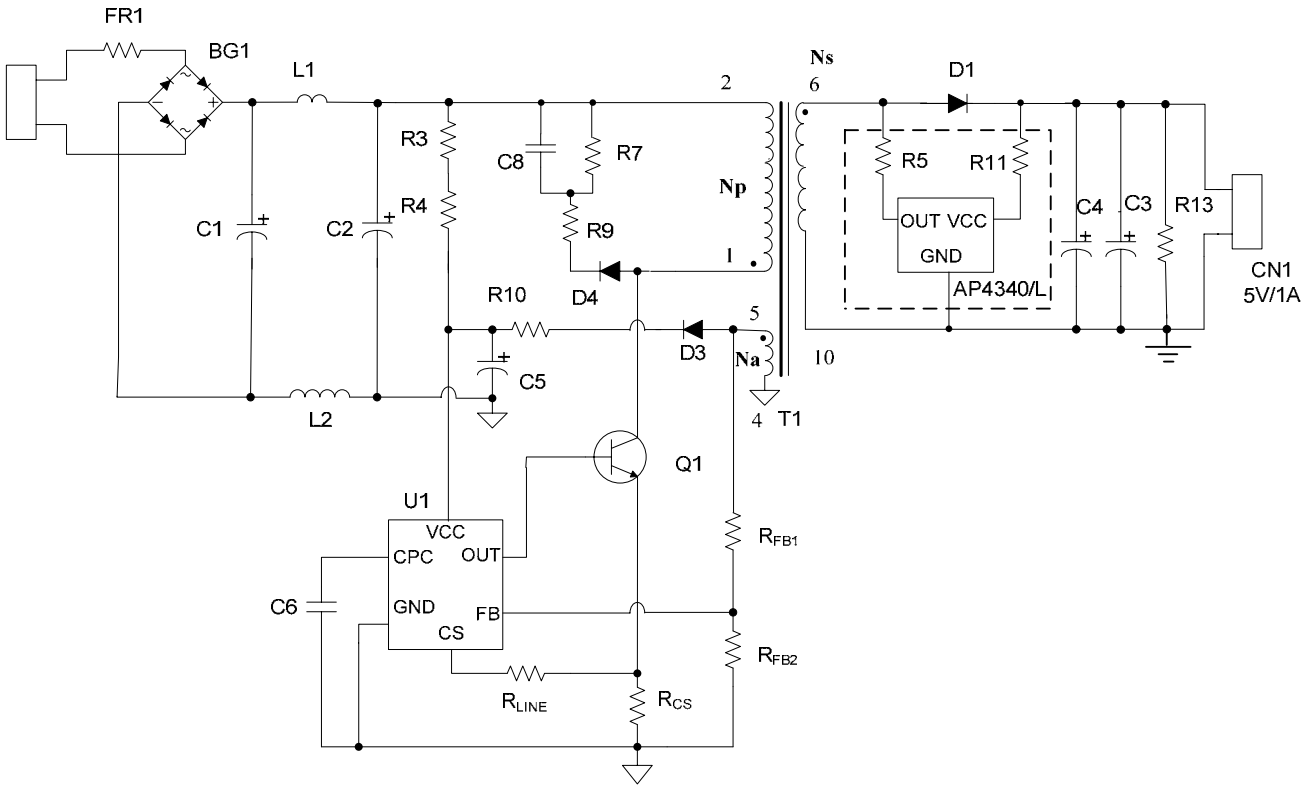

Figure 1. 5V/1A Output for Battery Charger of Mobile Phone

Figure 1 is typical application circuit with AP4340/L. VCC pin of AP4340/L is used to detect the system output voltage V_{OUT}. And OUT pin is used to provide the periodical signal under certain condition.

For some PSR system without AP4340/L, when load is changed from no load to heavy load, V_{OUT} will drop from 5V to somewhere below 4V at the worst case. If AP4340/L is applied in the secondary side, when V_{OUT} is detected below the internal trigger voltage (V_{TRI} in Figure 2), the OUT pin of AP4340/L will output a periodical pulse (t_{OSC} in Figure 2). Then PSR controller will receive the coupled pulse through transformer, and trigger the controller to turn on primary switch to respond the lower output condition and prevent V_{OUT} dropping any more.

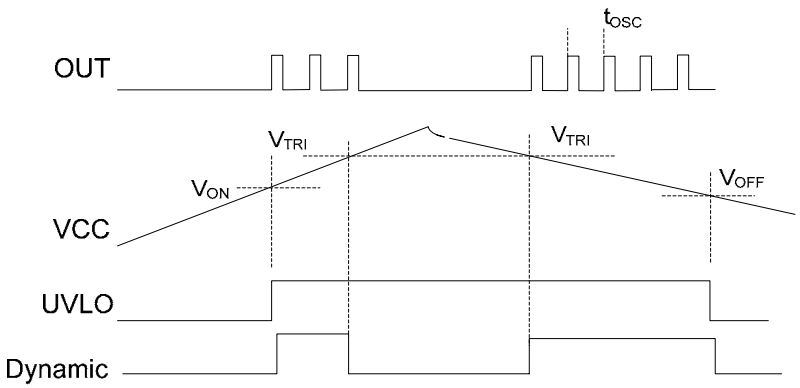

Figure 2. Typical Waveforms of AP4340/L

Besides working at dynamic moments, the AP4340/L can also work at steady status condition with no load or very light load. The highest switching frequency is determined by t_{ONP}, t_{ONS} and t_D($f_{sw\_4340} = \frac{1}{t_{ONP} + t_{ONS} + t_D}$). Here, t_{ONP} and t_{ONS} are parameters of system. t_D is parameter of PSR controller. So, at very light load, the AP4340/L will improve the CV precision.

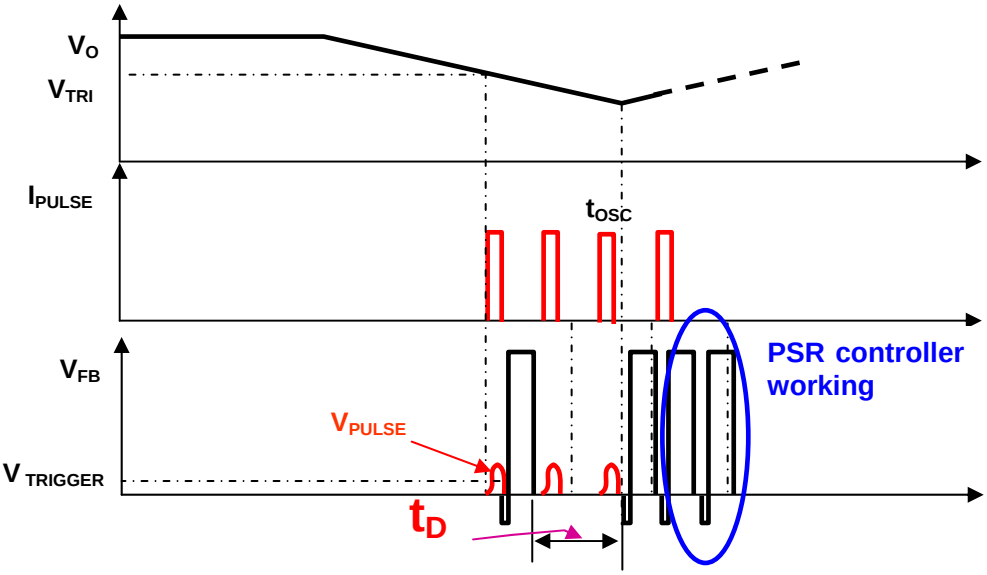

Figure 3. The Principle of AP4340/L and PSR Controller

The detailed operation waveform is shown in Figure 3. When AP4340/L detects the output voltage is lower than V_{TRI}, a pulse current (I_{PULSE}) will be generated. Then, a pulse voltage (V_{PULSE}) can be seen on the feedback winding coupling from the transformer. When PSR controller detects V_{PULSE} (>$V_{TRIGGER}$ is valid), it will provide a primary switch turn on signal for the primary side. V_{PULSE} will be valid again after a delay time (t_D), which is determined by PSR controller. Any V_{PULSE} in t_D is invalid, which can avoid any false triggering.

Note 1--- Avoiding False Triggering

There is a ringing signal on FB waveform after Schottky diode current decrease to zero, which is caused by magnetizing inductance and equivalent output capacitance of primary switch. PSR controller can't distinguish the ring signal and V_{PULSE} generated by AP4340/L. The delay time t_D is set to avoid PSR controller false triggering as to such ring signal. So the peak value of ring voltage should be much less than $V_{TRIGGER}$ after t_D in the design. Otherwise, V_{OUT} at no-load and extra-light load will get out of regulation.

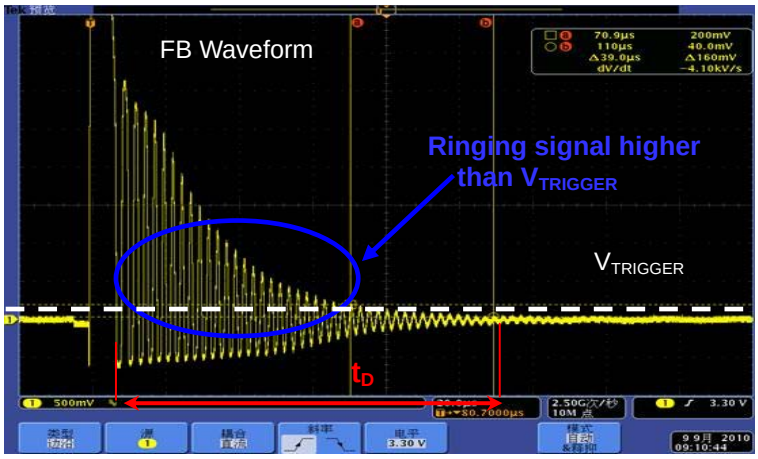

Figure 4. The Ring Signal of FB Pin

Note 2--- ESD Capability

The method of strengthen the ESD capability of system is to add two resistors (R5 and R11 in Figure 1) at OUT and VCC of AP4340/L. The value of each resistor is suggested to be between 30Ω and 100Ω. The higher resistance will weaken the I_{PULSE} of AP4340/L, which will cause missing trigger signal and the worse undershoot voltage. In the other side, the higher resistance will make bigger voltage at R11 which will decrease the VCC voltage of AP4340/L. If $VCC=V_{OUT}-V_{R11}$ is lower than the power-off voltage, the AP4340/L will stop working. The package of these two resistors should be bigger than 0805.

At the same time, the PCB layout of AP4340/L and peripheral devices should be paid more attention. The traces (Green lines in Figure 5) from AP4340/L's VCC, OUT and GND should be separated and avoided overcrossing.

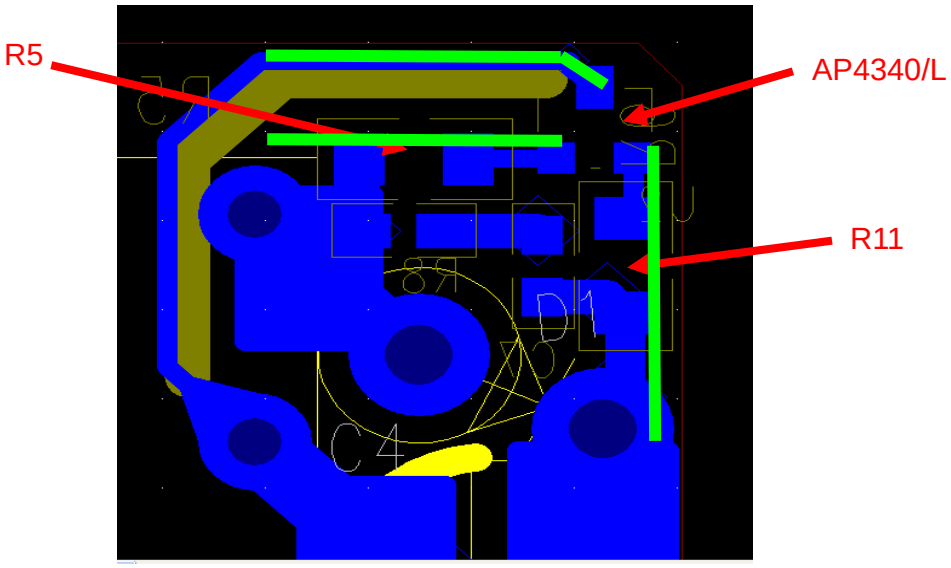

Figure 5. PCB Layout of AP4340/L and Peripheral Devices