Design Consideration with AP3581A/B/C and AP3583/A

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1. Introduction

The AP3581A/B/C and AP3583/A are voltage-mode single phase synchronous buck controllers with embedded MOSFET drivers. The AP3581A/BC and AP3583/A operate at fixed frequency of 300kHz (AP3581A/B, AP3583A) or 200kHz (AP3581C, AP3583). The reference voltage is 0.8V (AP3581B/C) and 0.6V (AP3581A, AP3583/A). The main difference between AP3581A/B/C and AP3583/A is that: the AP3583/A has an internal compensation, and it supports both tracking mode and stand-alone mode operation. The output voltage is tightly regulated to the external reference voltage from 0.4V to 3V at tracking mode or internal 0.6V reference at stand-alone mode.

2. Functional Description

The AP3581A/B/C and AP3583/A include internal soft-start and pre-biased output, power input detection, over voltage protection, under voltage protection, over current protection and shutdown function. They provide customers a compact, high efficiency, well-protected and cost-effective solutions. For more information, please refer to the functional block diagram (Figure 1 and 2).

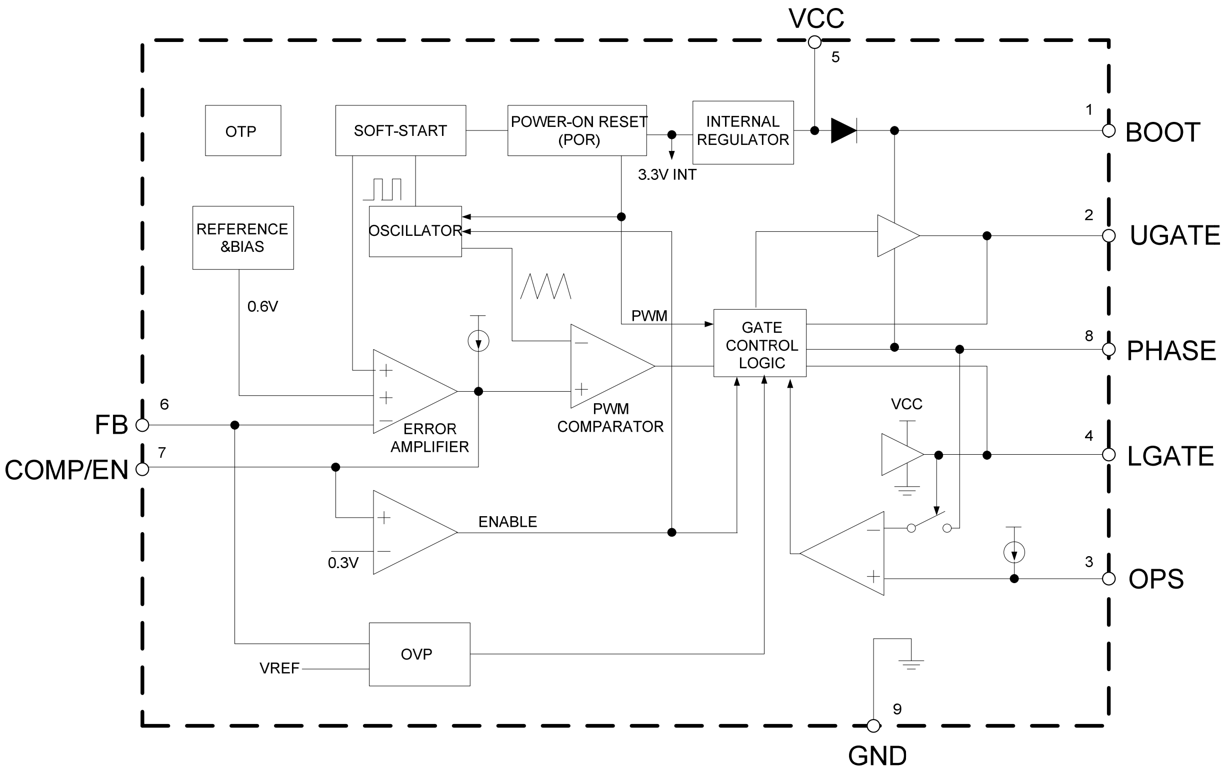

Figure 1. Functional Block Diagram of AP3581A/B/C

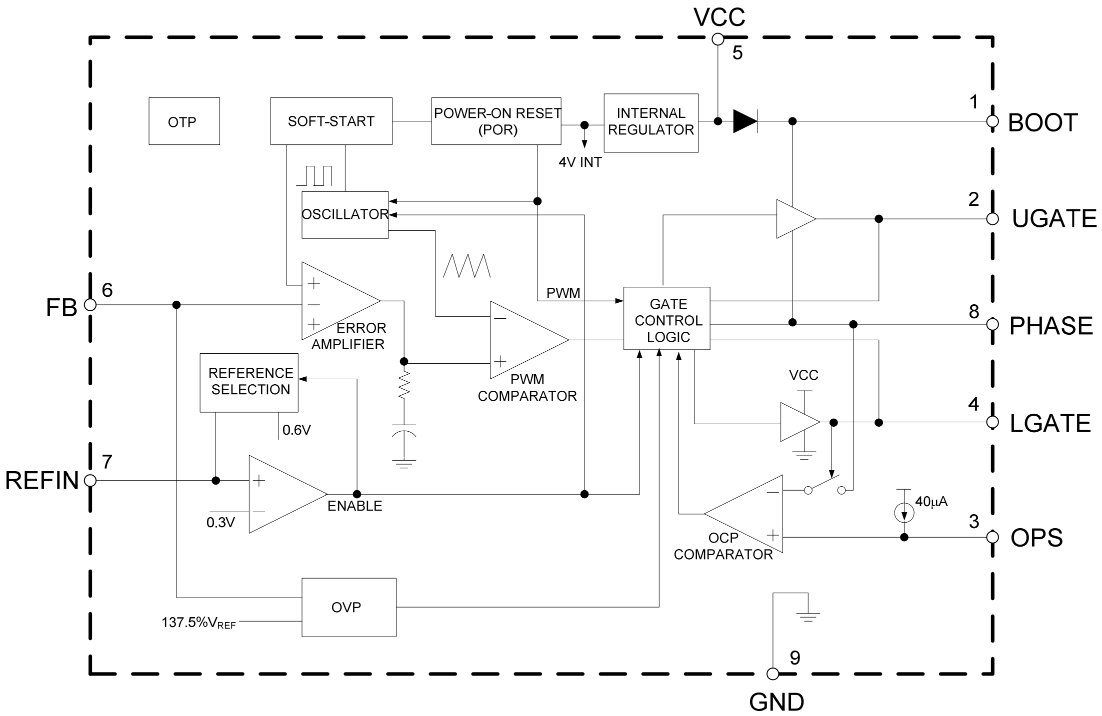

Figure 2. Functional Block Diagram of AP3583/A

2.1 Power on Reset and Chip Enable

A Power On Reset (POR) circuitry continuously monitors the supply voltage at VCC pin. Once the rising POR threshold is exceeded, the AP3581A/B/C and AP3583/A set themselves to active state and are ready to accept chip enable command. The rising POR threshold is typically 4.2V at V_{CC} rising.

For AP3581A/B/C, the COMP/EN is a multifunctional pin: control loop compensation and chip enable as shown in Figure 3. An Enable Comparator monitors the COMP/EN pin voltage for chip enable. A signal level transistor is adequate to pull this pin down to ground and shut down AP3581A/B/C. A 120μA current source charges the external compensation network with 0.45V ceiling when this pin is released. If the voltage at COMP/EN pin exceeds 0.3V, the AP3581A/B/C initiates its soft-start cycle.

The 120μA current source keeps charging the COMP pin to its ceiling until the feedback loop boosts the COMP pin higher than 0.45V according to the feedback signal. The current source is cut off when V_{COMP} is higher than 0.45V during normal operation.

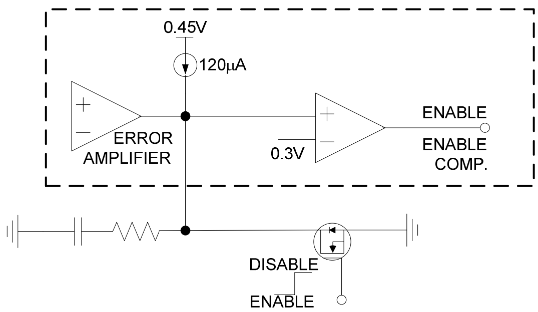

Figure 3. Chip Enable (AP3581A/B/C)

For AP3583/A, The REFIN is a multifunctional pin: external reference input and chip enable as shown in Figure 4.

To select internal 0.6V reference voltage, just let REFIN pin open. A 100μA current source tries to pull high the REFIN voltage after POR is detected by the enable comparator. An signal level transistor is adequate to pull this pin down to ground and shut down the AP3583/A. As Q1 turns off, the REFIN voltage is pulled high to V_{DD} by the 100 μA current source. As the REFIN voltage acrosses 0.3V threshold, the enable comparator initiates the operation of the AP3583/A. The REFIN voltage is compared with 3.0V voltage to select the reference voltage with 1ms delay after chip enabling. The internal 0.6V reference voltage is selected. Soft-start cycle is initiated after reference selection is completed.

To select external reference voltage, connect REFIN to a voltage ranging from 0.4V to 3V. As Q1 is turned off, the REFIN voltage is aligned to the external reference input. As the REFIN voltage acrosses 0.3V threshold, the enable comparator initiates the operation of AP3583/A. The REFIN voltage is compared with 3.0V voltage to select the reference voltage with 1ms delay after chip enabling. The external reference input is selected as the reference voltage when REFIN voltage is lower than 3.0V. If the reference input voltage is higher than 3.0V, the internal 0.6V reference voltage is still be selected. Soft-start cycle is initiated after reference selection is completed

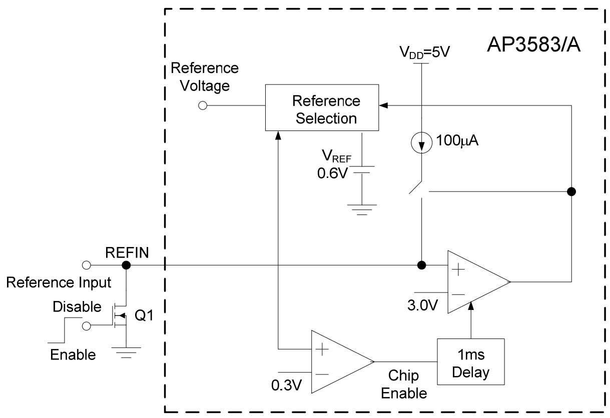

Figure 4. Chip Enable and Reference Selection (AP3583/A)

2.2 Soft-start

A built-in soft-start is used to prevent surge current from power supply input V_{IN} during turning on (Refer to the Functional Block Diagram). The error amplifier is a three-input device. Reference voltage V_{REF} or the internal soft-start voltage SS whichever is smaller dominates the behavior of the non-inverting inputs of the error amplifier. SS internally ramps up to 0.6V in 2.0ms for AP3581A /AP3583A (to 0.6V in 2.6ms for AP3583; to 0.8V in 2.7ms for AP3581B; to 0.8V in 3.6ms for AP3581C) after the soft-start cycle is initiated. The ramp is created digitally, so there will be 100 small discrete steps. Accordingly, the output voltage will follow the SS signal and ramp up smoothly to its target level.

The SS signal keeps ramping up after it exceeds the internal 0.6V (AP3581A, AP3583/A) or 0.8V (for AP3581B/C) reference voltage. However, the internal 0.6V or 0.8V (for AP3581B/C) reference voltage takes over the behavior of error amplifier after $V_{SS}>V_{REF}$. When the SS signal climb to its ceiling voltage (4.2V), the AP3581A/B/C and AP3583/A claims the end of soft-start cycle and enable the under voltage protection of the output voltage.

Figure 5 shows a typical start-up interval for AP3581A/B/C where the COMP/EN pin has been released from a grounded (system shutdown) state. The internal 120μA current source starts charge the compensation network after the COMP/EN pin is released from ground at T1. The COMP/EN exceeds 0.3V and enables the AP3581 at T2. The COMP/EN continues ramping up the stays at 0.45V before the SS starts ramping at T3. The output voltage follows the internal SS and ramps up to its final level during T3 and T4. At T4, the reference voltage V_{REF} takes over the behavior of the error amplifier as the internal SS crosses V_{REF}. The internal SS keeps ramping up and stay at 4.2V at T5, where AP3581 asserts the end of soft-start cycle.

Figure 6 shows a typical start-up waveform of AP3581 for VIN powering on.

For the external reference voltage of AP3583/A, the effective soft-start time is calculated as:

$t_{SS}=2.5\times V_{REF}$(ms)

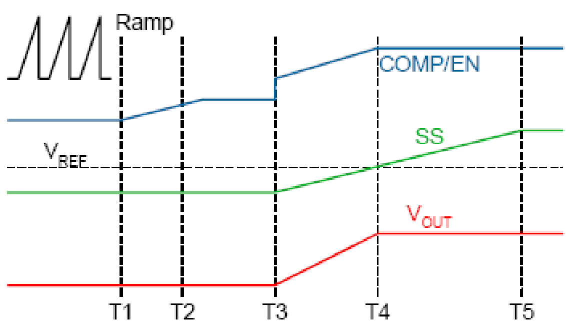

Figure 5. Start-up Interval

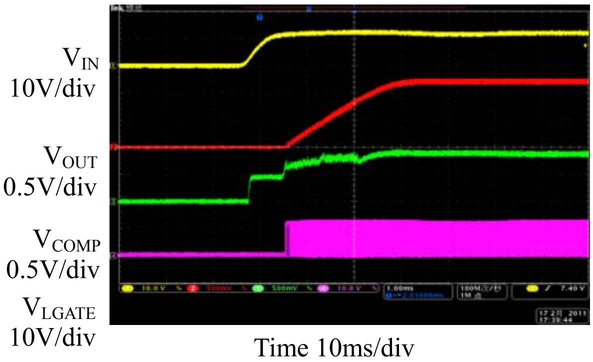

Figure 6. Start-up Waveform of AP3581A/B/C

2.3 Pre-Biased Outputs

Figure 7 shows the normal V_{OUT} start-up curve in blue; Initialization begins at T0, and output ramps between T1 and T2. If the output is pre-biased to a voltage less than the expected value, as shown by the magenta curve, the AP3581A/B/C and AP3583/A will detect that condition. Neither MOSFET will turn on until the soft-start ramp voltage exceeds the output; V_{OUT} starts seamlessly ramping from there. If the output is pre-biased to a voltage above the expected value, as in the black curve, neither MOSFET will turn on until the output voltage is pulled down to the expected value through external load. Any resistive load connected to the output will help pull down the voltage.

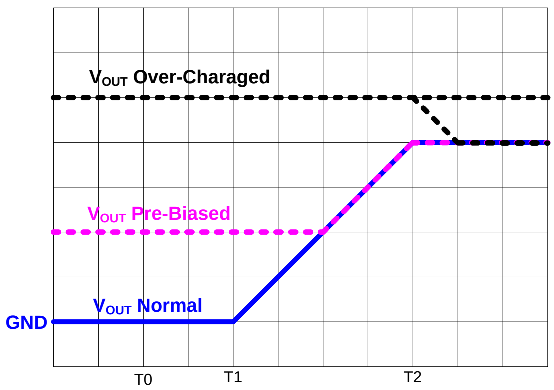

Figure 7. Soft-start with Pre-bias

2.4 Power Input Detection

The AP3581A/B/C and AP3583/A detect PHASE voltage for the present of power input V_{IN} when UGATE turns on the first time. If the PHASE voltage does not exceed 2.0V when UGATE turns on, the AP3581A/B/C asserts that V_{IN} is not ready and stops the soft-start cycle. However, the internal SS continues ramping up to VDD. Another soft-start is initiated after SS ramps up to VDD. The hiccup period is about 1ms. Figure 8 shows the start-up waveform where V_{IN} does not present initially.

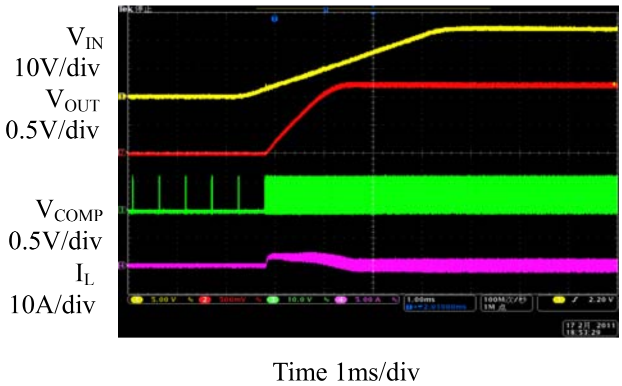

Figure 8. Soft-start (V_{IN} not Present Initially)

2.5 Over Current Protection (OCP)

Figure 9 shows the over current protection (OCP) scheme of AP3581A/B/C and AP3583/A. A resistor R_{OCSET} connected from OPS pin sets the threshold. An internal current source I_{OC} (40μA typically), flowing through R_{OCSET} determines the OCP trigger point I_{OCSET}, which can be calculated using the following equation:

$$I_{OCSET} = \frac{40\mu A \times R_{OCSET}}{10 \times R_{DS(ON)\_L}}$$

Where $R_{DS(ON)\_L}$ is the $R_{DS(ON)}$ of the low side MOSFET. Because the $R_{DS(ON)}$ of MOSFET increases with temperature, it is necessary to take this thermal effect into consideration in calculating OCP point.

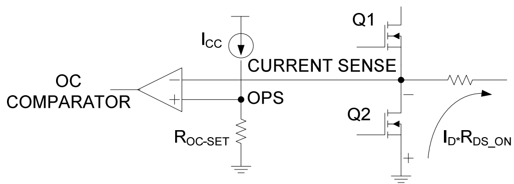

Figure 9. Over Current Protection Scheme

When OCP is triggered, both UGATE and LGATE will go low to stop the energy transferred to the load. The controller will try to restart in a hiccupped way. Figure 10 shows the hiccupped over current protection. Only four times of hiccup is allowed in over current. If over current protection still exist after four times of hiccup, controller will be latched.

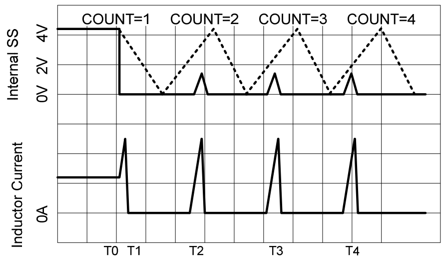

Figure 10. Hiccupped Over Current Protection

2.6 Over Voltage Protection (OVP)

The feedback voltage is continuously monitored for over voltage protection. When OVP is triggered, LGATE will go high and UGATE will go low to discharge the output capacitor.

The AP3581A/B/C and AP3583/A provide full-time over voltage protection whenever soft-start completes or not. The typical OVP threshold is 137.5% of the internal reference voltage V_{REF}. The AP3581A/B/C and AP3583/A provide non-latched OVP. The controller will return to normal operation if over voltage condition is removed.

2.7 Under Voltage Protection (UVP)

The feedback voltage is also monitored for under voltage protection. The UV threshold is set at 0.4V. The under voltage protection has 15μs triggered delay. When UVP is triggered, both UGATE and LGATE will go low. Unlike OCP, UVP is not a latched protection; The controller will always try to restart in a hiccupped way.

2.8 Thermal shutdown

If the junction temperature of the device reaches the thermal shutdown limit of 160°C, the PWM and the oscillator is turned off and UGATE and LGATE are driven low, turning off both MOSFETs. When the junction cools to the required level (140°C nominal),

2.9 Output Voltage Selection

The output voltage can be programmed to any level between the 0.6V internal reference (0.8V for AP3581B/C) to the 80% of V_{IN} supply. The lower limitation of output voltage is caused by the internal reference. The upper limitation of the output voltage is caused by the maximum available duty cycle (80%). This is to leave enough time for over current detection. Output voltage out of this range is not allowed.

A voltage divider sets the output voltage (Refer to the typical application circuit). In real applications, choose R1 in 100Ω to 10kΩ range and choose appropriate R2 according to the desired output voltage.

For AP3581A and AP3583/A,

$$V_{OUT} = 0.6V \times \frac{R1 + R2}{R1}$$

For AP3581B/C,

$$V_{OUT} = 0.8V \times \frac{R1 + R2}{R1}$$

3. Component Selection

Typical application circuit of AP3581A/B/C and AP3583/A are shown in Figure 11 and 12. For the buck controller, the major external components are power MOSFET switches, output inductor, input capacitor and output capacitor. The selection of external component is primarily determined by the maximum load current and begins with the selection of power MOSFET switches. The desired amount of ripple current and operating frequency largely determines the inductor value. Finally, input capacitor is selected for its capability to handle the large RMS current and output capacitor is chosen with low enough ESR to meet the output voltage ripple and transient specification.

3.1 Power MOSFET Selection

The AP3581A/B/C and AP3583/A require 2 N-channel power MOSFET for upper (controlled) and lower (synchronous) switches. These should be selected based on $R_{DS(ON)}$, gate supply requirements, and the thermal management requirements

The gate drive voltage is supplied by VCC pin that receives 4.5 to 13.2V supply voltage. When operating with a 7~13.2V power supply for VCC, a wide variety of N-MOSFET can be used. Logic-level threshold MOSFET should be used if the input voltage is expected to drop below 7V. Caution should be exercised with devices exhibiting very low $V_{GS(ON)}$ characteristics.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components: conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFET. These losses are distributed between the two MOSFETs ac-

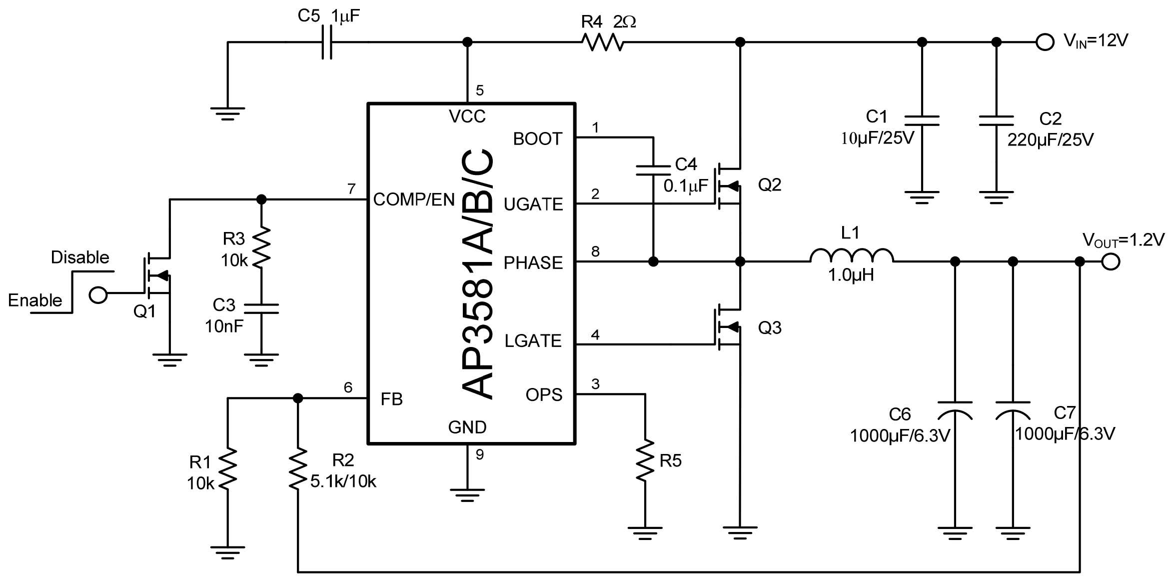

Figure 11. Typical Application of AP3581A/B/C

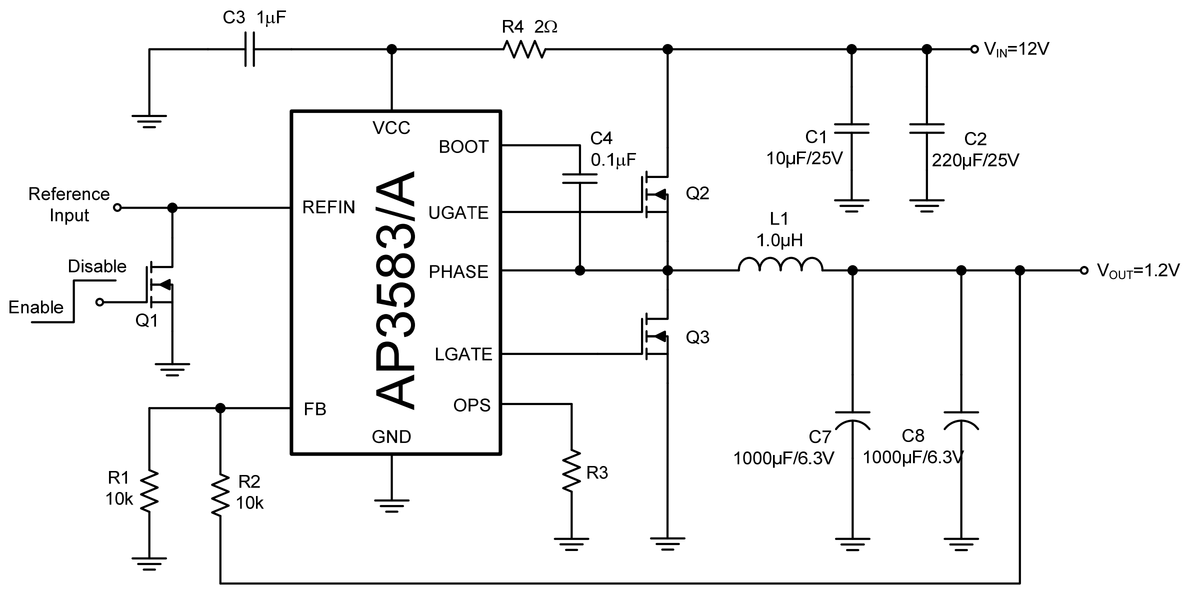

Figure 12. Typical Application of AP3583/A

cording to duty cycle. Since the AP3581A/B/C and AP3583/A are operating in continuous conduction mode, the duty cycle is:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The resulting power dissipation in the MOSFET at maximum output current are:

$$P_{UP} = I_{OUT}^2 \times R_{DS(ON)} \times D + \frac{1}{2} \times I_{OUT} \times V_{IN} \times T_{SW} \times f_S$$

$$P_{LOW} = I_{OUT}^2 \times R_{DS(ON)} \times (1 - D)$$

Where t_{SW} is the combined switch ON and OFF time, and f_S is the switching frequency.

Both MOSFETs have I^2R losses and the upper MOSFET includes an additional term for switching losses, which are largest at high input voltages. The lower MOSFET losses are greatest when the duty cycle is near 0, during a short-circuit or at high input voltage. These equations assume linear voltage current transitions and do not adequately model power loss due the reverse-recovery of the lower MOSFET's body diode.

Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

The gate-charge losses are mainly dissipated by the AP3581A/B/C and AP3583/A and don't heat the MOSFETs. However, large gate charge increases the switching interval, T_{SW} that increases the MOSFET switching losses. The gate-charge losses are calculated as:

$$P_G = V_{CC} \times (V_{CC} \times (C_{ISS\_UP} + C_{ISS\_LOW}) + V_{IN} \times C_{RSS\_UP}) \times f_S$$

Where C_{ISS_UP} and C_{ISS_LOW} are the input capacitance of the upper and lower MOSFET, and C_{RSS_UP} is the reverse transfer capacitance of upper MOSFET. Make sure that the gate-charge loss will not cause over temperature at AP3581A/B/C and AP3583/A, especially with large gate capacitance and high supply voltage.

3.2 Output Inductor Selection

Output inductor selection is usually based on the consideration of inductance, rated current, size requirements and DC resistance (DCR). The inductor value relies on the switching frequency, load current, ripple current and duty cycle.

A higher-value inductor can decrease the ripple current and output ripple voltage, however usually with larger physical size. And the large inductor value reduces the converter's response time to a load transient. So some compromise needs to be made when selecting the inductor. In most applications, a good compromise is choosing the ripple current that is 20% of $I_{OUT(MAX)}$. And the inductance L can be selected according to:

$$L = V_{OUT} \times \frac{V_{IN} - V_{OUT}}{f_S \times V_{IN} \times I_{OUT} \times 20\%}$$

Another important parameter for selecting the inductor is the current rating. After fixing the inductor value, the peak inductor current can be expressed as:

$$I_{PEAK} = I_{OUT} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times V_{IN} \times f_S \times L}$$

The current rating of the selected inductor should be ensured to be 1.5 times of the peak inductor current.

The size requirements refer to the area a height requirement for a particular design. For better efficiency, choose a low DC resistance inductor. DCR is usually inversely proportional to size.

3.3 Output Capacitor Selection

The selection of output capacitor is primarily determined by the ESR (Effective Series Resistance) required to minimize voltage ripple and load step transients. The output ripple ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} = \Delta I_L \times \left(R_{ESR} + \frac{1}{8 \times C_{OUT} \times f_S} \right)$$

Where ΔI_L is the inductor ripple current, and R_{ESR} is ESR of output capacitor.

The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout. Modern components and loads are capable of producing transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components.

Use only special low-ESR capacitors intended for switching regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes.

3.4 Input Capacitor Selection

The synchronous-rectified Buck converter draws pulsed current with sharp edges from the input capacitor, resulting in ripples and spikes at the input supply voltage. Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time upper MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs to avoid the stray inductance along the connection trace.

The important parameters for the input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck converter is calculated as:

$$\mathrm{I_{CIN\_RMS}} = I_{OUT(MAX)} \times \sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN}}}$$

3.5 OCP Resistor $\mathrm{R_{OCSET}}$ Setting

The OCP triggering point $\mathrm{I_{OCSET}}$ follows the valley detection of inductor current. For a certain application condition, the valley inductor current can be expressed as:

$$\mathrm{I_{VALLEY}} = I_{OUT} - \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times V_{IN} \times f_S \times L}$$

Considering the temperature effect of MOSFET $\mathrm{R_{DS(ON)}}$, internal current source $\mathrm{I_{OC}}$ difference and precision of resistor $\mathrm{R_{OCSET}}$, the OCP trigger point $\mathrm{I_{OCSET}}$ should be set above about 15% to 20% $\mathrm{I_{VALLEY}}$ for enough margin. So the OCP resistor $\mathrm{R_{OCSET}}$ can be set as:

$$\mathrm{R_{OCSET}} = \frac{[(1 + 15\%\ \text{to}\ 20\%) \times \mathrm{I_{VALLEY}}] \times 10 \times \mathrm{R_{DS(ON)\_L}}}{40\mu\mathrm{A}}$$

3.6 Feedback Loop Compensation

Figure 13 highlights the voltage-mode control loop for a synchronous-rectified buck converter consisting of AP3581 (AP3583 has the internal compensation). The control loop includes two stages: Modulator and Power stage & Sensor and Compensation stage.

The modulator transfer function is the small-signal transfer function of $\mathrm{V_{OUT}/V_{COMP}}$. This function is dominated by a DC gain and the output filter (L and $\mathrm{C_{OUT}}$), with a double pole break frequency at $\mathrm{f_{LC}}$ and a zero at $\mathrm{f_{ESR}}$. The DC gain of the modulator is simply the input voltage ($\mathrm{V_{IN}}$) divided by the peak-to-peak oscillator voltage $\mathrm{V_{OSC}}$.

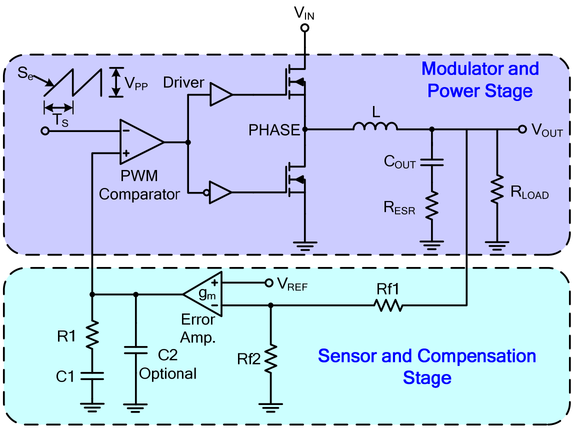

Figure 13. Voltage Control Loop Using AP3581

The output LC filter introduces a double pole, 40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180 degrees. The double pole of the LC filter is expressed as:

$$f_{LC} = \frac{1}{2\pi \cdot \sqrt{L \times C_{OUT}}}$$

The ESR zero is contributed by the ESR associated with the output capacitor. The ESR zero of the output capacitor is expressed as:

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}$$

Figure 14 illustrates the bode plot of power and modulator using AP3581A/B/C and AP3583/A.

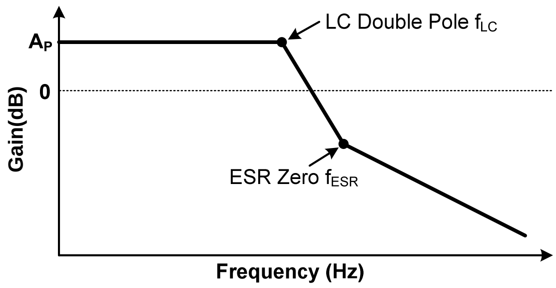

Figure 14. Power and Modulator Bode Plot

The AP3581A/B/C and AP3583/A adopt operational transconductance amplifier (OTA) as the error amplifier. Figure 15 shows a type II compensation network using OTA, which provides two poles and one zero to the control loop.

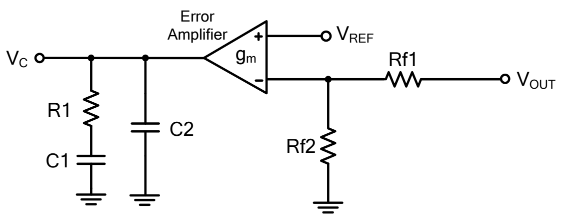

Figure 15. Type II Compensation Network Using OTA

The compensator transfer function is the small-signal transfer function of V_C/V_{OUT}. This function is dominated by the Mid-Band gain and compensation zero and pole. The Mid-band gain of the compensation is expressed as:

$$Mid\_Band\_Gain = \frac{R1}{R_{f1}} \times g_M$$

One of the poles is located at low frequency to increase the low frequency gain to improve the DC regulation accuracy. The location of the other pole and the single zero can be calculated as follows:

$$f_Z = \frac{1}{2\pi \times R1 \times C2}$$

$$f_P = \frac{1}{2\pi \times R_1 \times \left(\frac{C_1 \times C_2}{C_1 + C_2}\right)}$$

Figure 16 illustrates the system bode plot. The open loop gain is the sum of the modulation gain and the compensation gain. The goal is to obtain the required crossover frequency with sufficient phase margin. The preferred phase margin is greater than 45°. Follow the guidelines for locating the poles and zeros of the compensation network.

1) Pick Mid-Band gain(R_1) for desired crossover frequency, which is preferred to be 1/10 to 1/5 of the switching frequency;
2) Place compensation zero $f_Z(C_1)$below LC double pole(25%f_{LC});
3) Place compensation pole $f_P(C_2)$at half of the switching frequency;
4) Check the system open loop gain;
5) Estimate phase margin, repeat if necessary.

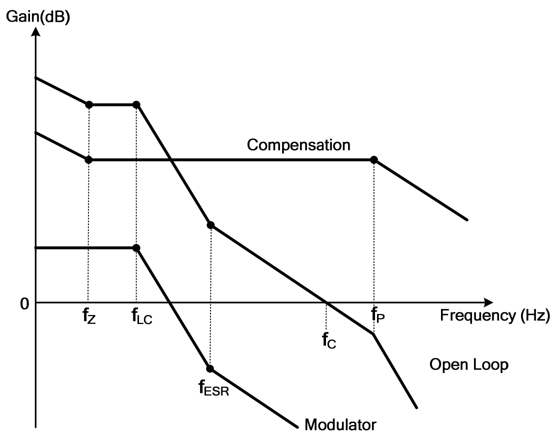

Figure 16. System Bode Plot

4. PCB Layout Considerations

High speed switching and relatively large peak currents in a synchronous-rectified buck converter make the PCB layout a very important part of design. Switching current from one power device to another can generate voltage spikes across the impedances of the interconnecting bond wires and circuit traces. The voltage spikes can degrade efficiency and radiate noise, that results in over-voltage stress on devices. Careful component placement layout an printed circuit design can minimize the voltage spikes induced in the converter.

Follow the below layout guidelines for optimal performance of the AP3581A/B/C and AP3583/A.

1) The turn-off transition of the upper MOSFET prior to turn-off, the upper MOSFET was carrying the full load current. During turn-off, current stops flowing in the upper

MOSFET and is picked up by the low side MOSFET. Any inductance in the switched path generates a large voltage spike during the switching interval. Careful component selections, layout of the critical components, and use shorter and wider PCB traces help in minimizing the magnitude of voltage spikes.

2) The power components and the PWM controller should be placed firstly. Place the input capacitors, especially the high-frequency ceramic decoupling capacitors, close to the power switches. Place the output inductor and output capacitors between the MOSFETs and the load. Also locate the PWM controller near by the MOSFETs.

3) Use a dedicated grounding plane and use vias to ground all critical components to this layer. Use an immediate via to connect the component to ground plane including GND of the AP3581A/B/C and AP3583/A.

4) Apply another solid layer as a power plane and cut this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the PHASE node.

5）The PHASE node is subject to very high dV/dt voltages. Stray capacitance between this island and the surrounding circuitry tend to induce current spike and capacitive noise coupling. Keep the sensitive circuit away from the PHASE node and keep the PCB area small to limit the capacitive coupling. However, the PCB area should be kept moderate since it also acts as main heat convection path of the lower MOSFET.

6）The PCB traces between the PWM controller and the gate of MOSFET and also the traces connecting source of MOSFETs should be sized to carry 2A peak currents.