Design Guideline and Application Notes of AP1682 System Solution

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1. Introduction

The AP1682 is a high performance AC/DC universal input Primary Side Regulation Controller with Power Factor Correction for LED driver applications. The device uses Pulse Frequency Modulation (PFM) technology to regulate output current while achieving high power factor and low THD.

The AP1682 provides accurate constant current (CC) regulation while removing the opto-coupler and secondary control circuitry. It also eliminates the need of loop compensation circuitry while maintaining stability. The AP1682 achieves excellent regulation and high efficiency, yet meets the requirement of IEC61000-3-2 harmonic standard.

The AP1682 features low start-up current, low operation current and high efficiency. It also has rich protection features including over voltage, short circuit, over current, over temperature protection.

The AP1682 is available in SOIC-8 package.

2. Product Features

- Primary Side Control for Output Current Regulation Without Opto-coupler and Secondary CV/CC Control Circuitry
- Low Start-up Current
- High Power Factor and Low THD for Universal Input Range
- Tight CC Regulation Performance for Universal Input Mains Voltage Range
- Eliminates Control Loop Compensation Circuitry
- Wide VCC Voltage Range
- Built-in Acceleration Start
- Open-load and Reload Detection
- Over Voltage and Short Circuit Protection
- Over Temperature Protection
- Over Current Protection
- Cost Effective Total PFC LED Driver Solution

3. Pin Configuration and Description

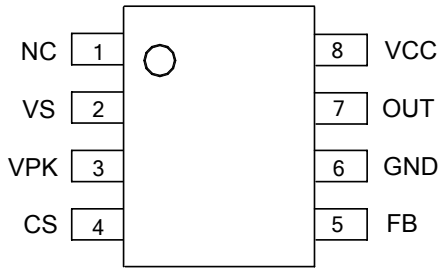

Figure 1. Pin Configuration of AP1682

Pin Number	Pin Name	Function
1	NC	No connection
2	VS	The rectified input voltage sensing pin. The pin is detecting the instantaneous rectified sine waveform of input voltage.
3	VPK	The rectified input voltage peak value sensing pin. The pin is detecting the rectified sine waveform peak value of input voltage.
4	CS	The primary current sense pin.
5	FB	This pin captures the feedback voltage from the auxiliary winding. FB voltage is used to control no load output voltage and determine acceleration stop point at start up phase.
6	GND	Ground. Current return for gate driver and control circuits of the IC.
7	OUT	Gate driver output pin.
8	VCC	Supply pin of gate driver and control circuit of the IC.

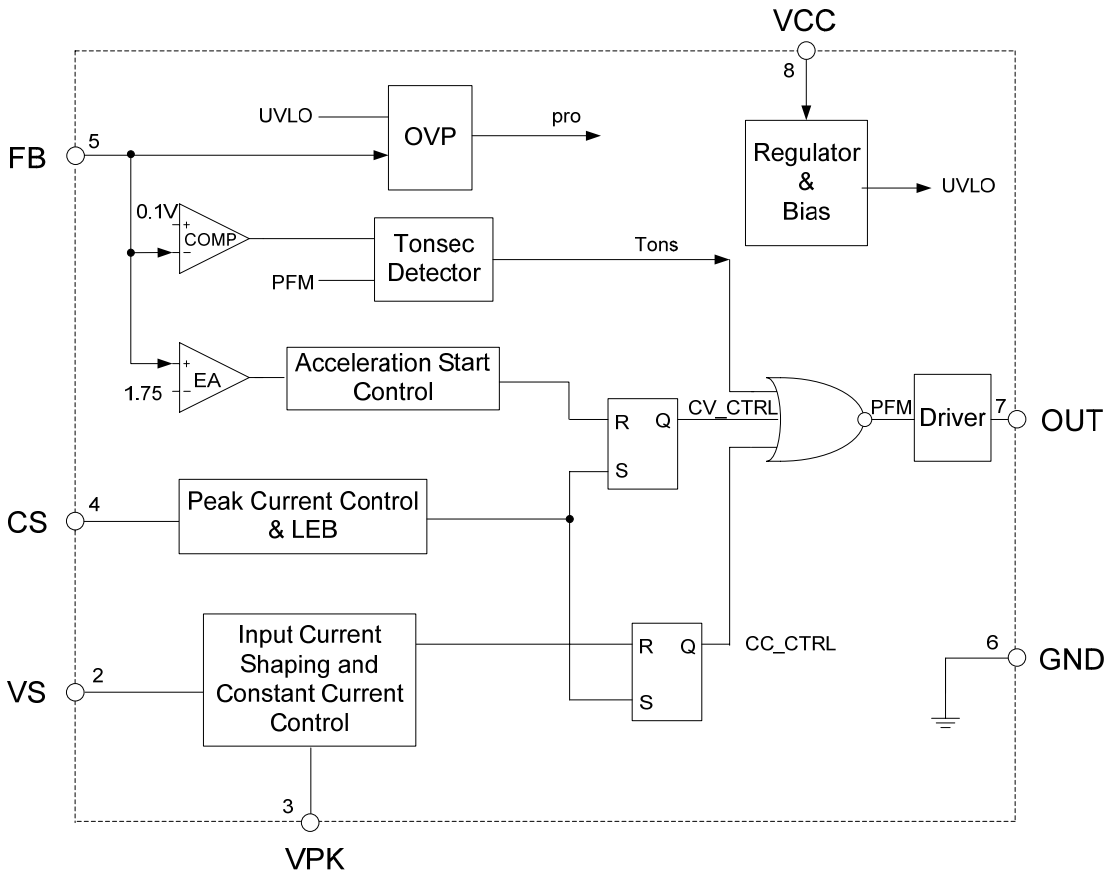

Figure 2. Functional Block Diagram of AP1682

4. Operation Principle Description

4.1 Power Factor Correction and Constant Output Current Control Strategy

The AP1682 uses Primary Side Regulation (PSR) to regulate constant output current and achieve the high Power Factor at the same time.

The function of PFC requires input AC current waveform to follow input AC voltage waveform, a sinusoidal waveform as we know.

The AP1682 solution uses PFM technology and Flyback converter always operates at Discontinuous Current Mode (DCM). So the input current I_{IN} is

$$I_{in}=\frac{I_{pk}\cdot T_{onp}}{2\cdot T_{sw}} \quad (1)$$

The primary switch on time T_{onp}, primary switch peak current I_{pk} and switching period T_{sw} are defined as:

$$T_{onp}=\frac{L_p\cdot I_{pk}}{V_{in}} \quad (2)$$

$$I_{pk}=\frac{V_{cs}}{R_{cs}} \quad (3)$$

$$T_{sw}=\frac{T_{ons}}{K} \quad (4)$$

Where, L_P is the primary winding magnetizing inductance of transformer, V_{CS} is the primary current sense voltage, R_{CS} is the current sense resistor, T_{ONS} is the conduction time of secondary side diode. From the above equations it can be got:

$$I_{in}=\frac{\frac{V_{cs}}{R_{cs}}\cdot\frac{L_p\cdot I_{pk}}{V_{in}}}{2\cdot\frac{T_{ons}}{K}}=\frac{\frac{V_{cs}}{R_{cs}}\cdot\frac{L_p}{V_{in}}\cdot\frac{V_{cs}}{R_{cs}}}{2\cdot\frac{T_{ons}}{K}}=\frac{L_p\cdot K\cdot V_{cs}^2}{2\cdot R_{cs}^2\cdot T_{ons}\cdot V_{in}} \quad (5)$$

The input AC voltage V_{IN} is defined

$$V_{in}=\sqrt{2}V_{in\_rms}\cdot\sin\theta \quad (6)$$

It is assumed that

$$V_{cs} = \frac{V_s}{V_{pk}} \cdot V_{CS\_REF} = K_{LINE} \cdot V_{CS\_REF} \cdot Sin\theta \quad (7)$$

$$K = \frac{T_{ons}}{T_{sw}} = K_{LINE} \cdot K_c \cdot Sin\theta \quad (8)$$

$$V_{CS,EQ} = V_{CS\_REF} \cdot K_c$$

Here, V_{CS_REF} is 1V, K_C is 4/9 and $V_{CS,EQ}$ is 4/9V. From the above equations, it can be obtained that

$$I_{in} = \frac{V_{out} \cdot N_t \cdot V_{CS,EQ} \cdot K_{LINE}^2}{2\sqrt{2} \cdot R_{cs} \cdot V_{in\_rms}} \cdot \sin\theta \quad (9)$$

So it can be seen that the input current follows the input voltage sinusoidal waveform, which shows PFC function works. Figure 3 shows the basic operation principle and waveforms of AP1682 PFC solution.

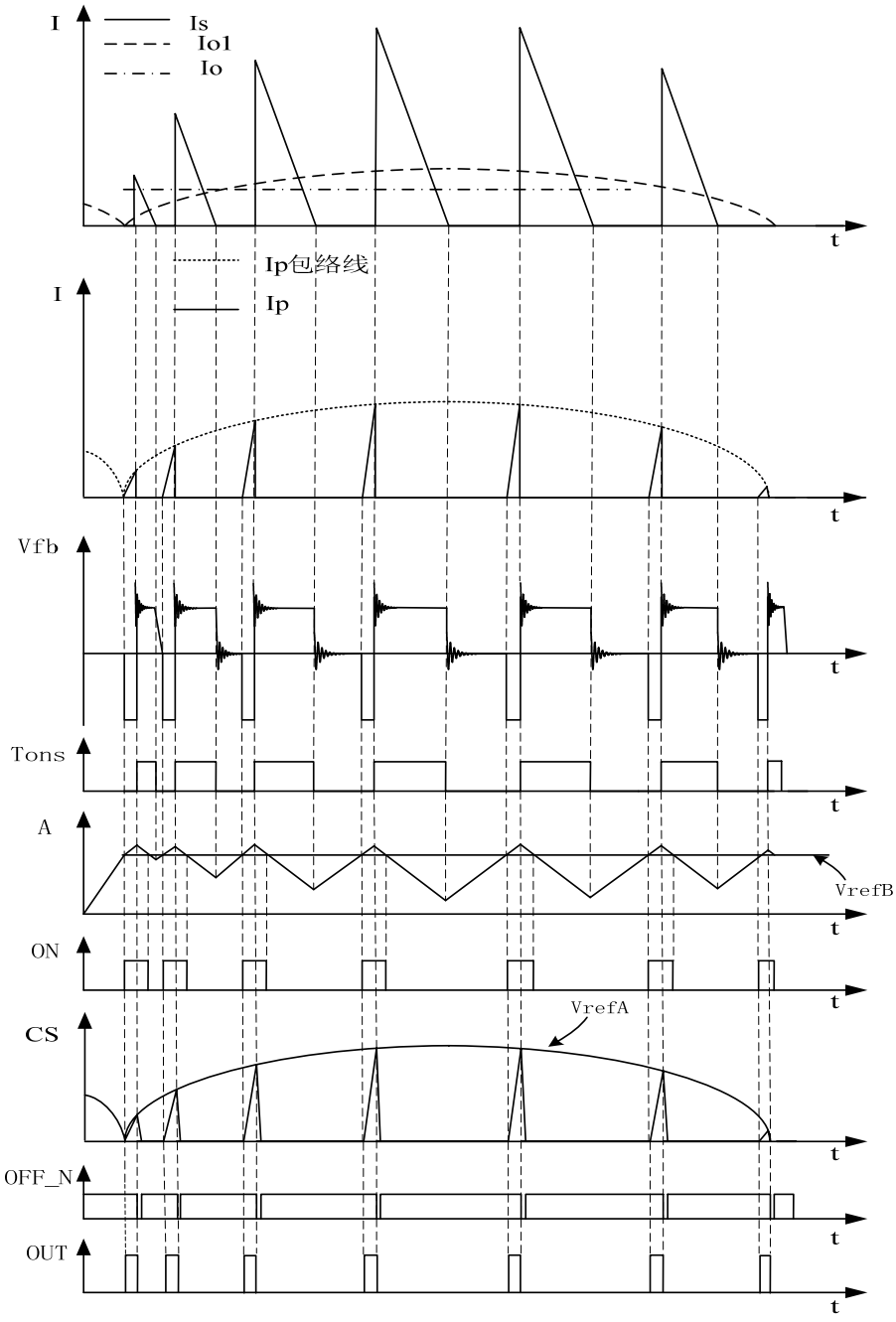

Figure 3. Basic Operation Waveforms

And the output current I_O can be got as

$$I_O = \frac{T_{ons}}{2 \cdot T_{sw}} \cdot I_{pks} = \frac{N_t \cdot T_{ons} \cdot V_{cs} \cdot \eta_t}{2 \cdot T_{sw} \cdot R_{cs}} = \frac{N_t \cdot V_{CS,EQ} \cdot K_{LINE}^2 \cdot \eta_t \cdot Sin^2\theta}{2 \cdot R_{cs}} = \frac{N_t \cdot V_{CS,EQ} \cdot K_{LINE}^2 \cdot \eta_t}{2 \cdot R_{cs}} \frac{1 - Cos2\theta}{2} \quad (10)$$

η_t is the power conversion efficiency considering the total power dissipation.

From above output current equation it is concluded that the output current has the double line frequency AC components, which results in the double line frequency output voltage and output current ripple. There are always output capacitors to filter the ripple in Flyback topology, so the output voltage ripple depends on the total output capacitance. And for LED driver, the output current ripple is determined by the output voltage ripple and LED loading V-I characteristics.

The output current DC value is

$$I_{o\_mean} = \frac{1}{\pi} \int_0^{\pi} \frac{N_t \cdot V_{CS,EQ} \cdot K_{LINE}^2 \cdot \eta_t \cdot Sin^2\theta}{2 \cdot R_{cs}} d\theta = \frac{N_t \cdot V_{CS,EQ} \cdot K_{LINE}^2 \cdot \eta_t}{4 \cdot R_{cs}} \quad (11)$$

Therefore, the constant output current control can be realized with appropriate parameter design.

4.2 Acceleration Start

For LED lighting application, the lower turn on delay time is required. To reduce start-up time, an acceleration start function is embedded in AP1682. At start-up phase, after VCC voltage reaches turn on threshold, AP1682 controls the power converter operating at the max frequency with DCM Boundary mode to provide more energy to output. The acceleration start phase will stop when detected FB pin voltage reaches soft start threshold 1.75V.

4.3 VCC Pin Voltage Region

In LED lighting application, because the LED cell forward voltage drop V_F varies with different current and operation temperature, the output voltage need a wider operation range. Therefore the VCC voltage which comes from aux winding coupling with transformer winding also needs the wider operating voltage range. The AP1682 start-up voltage threshold is 18.5V (typ.), and the UVLO voltage threshold is 8.0V. The AP1682 have a wide operating voltage window from 8V to 30V. If the VCC pin voltage is higher than 30V, the AP1682 will enter V_{CC} OVP protection state, which will lead to AP1682 automatic restart.

4.4 FB Pin Voltage Region

The FB pin voltage has several comparator thresholds for different function. At start-up phase, the AP1682 system works in acceleration start phase until FB pin voltage reaches 1.75V. From 1.75V to 4V, the system works in CC region. The output current is constant regardless of output voltage changing. When open load condition or load disconnecting happens, the output voltage rises to the maximum value and the FB pin voltage reaches 4V. The system will work in HICCUP state to keep output voltage below the maximum value and VCC voltage changes between startup threshold and UVLO threshold. If abnormal condition happened such as fault connection or excess auxiliary winding turns, FB pin voltage reaches to 6V, then AP1682 will enter FB OVP protection state. This will lead to AP1682 latch working mode. Figure 4 shows the FB pin working regions.

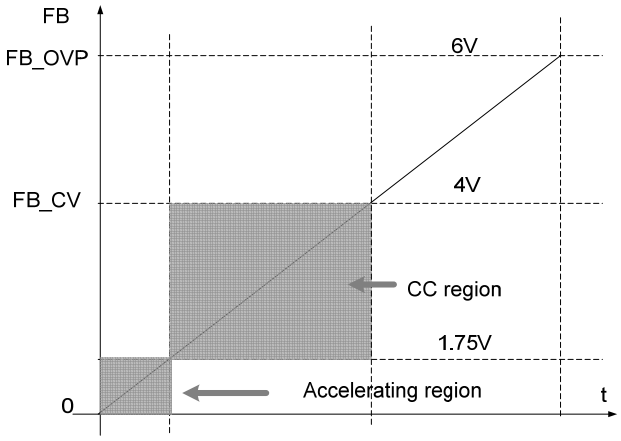

Figure 4. FB Function Region Diagram

4.5 Input Voltage Sensing

With the resistor divider circuit connecting to rectified DC bus, VS pin detects the instantaneous rectified sine waveform signal of input voltage and VPK pin detects the corresponding peak value. The internal divider by VS/VPK generates sine waveform as current reference signal. In general, the VS/VPK value should be design between 0 and 1.

4.6 Primary Current Sense and Over Current Protection (OCP)

The current sense signal connecting to CS pin is for primary peak current feedback and OCP function. The primary current sense resistor value is one of design inputs for output constant current value setting according to equation (13). The CS pin peak value at one half line cycle should be set as 1V. The primary OCP comparator

threshold is 4V for primary side short protection. When OCP threshold is triggered, AP1682 enters latch mode and switch stops working. The latch mode will be reset after input power recycle.

5. Operation Parameter Design and Components Selection

The off-line primary side regulation power factor solution with AP1682 is the single stage PFC Flyback structure. Since of PFC operation and the special PFM control technology, the circuit operation parameter of Flyback converter is little different with the traditional off-line Flyback converter. In a half line cycle, the operation parameters, such like DC bus voltage, primary peak current, duty cycle, etc., vary with input sine waveform voltage.

5.1 Transformer Turns Ratio Determination

In order to guarantee the Flyback converter operating at DCM mode at the whole input range and output loading condition, the Tons, Tonp and Tsw should meet

$$T_{ons} + T_{onp} < T_{sw} \tag{12}$$

According to the PFM principle, at the minimum input voltage $V_{IN\_RMS\_MIN}$ and the maximum output power (the maximum output voltage V_{O_MAX} and constant output current I_O) condition, the Flyback converter with AP1682 operates at the closest to DCM boundary mode. So from the equation (10) it can be get

$$\frac{L_p \cdot I_{pk}}{\sqrt{2} \cdot V_{in\_rms\_min}} + \frac{L_s \cdot I_{pks}}{V_{o\_max} + V_d} < \frac{L_s \cdot I_{pks}}{V_{o\_max} + V_d} \cdot \frac{1}{K_c \cdot K_{LINE}} \tag{13}$$

Where V_d isthe voltage drop on the secondary diode and trace resistance. From the transformer relationship between primary parameter and secondary parameter, it can be got:

$$N_t < \left(\frac{1}{K_c \cdot K_{LINE}} - 1 \right) \cdot \frac{\sqrt{2} \cdot V_{in\_rms\_min} \cdot \eta_t}{V_{o\_max} + V_d} \tag{14}$$

The final turn ratio design should also be revised by considering the primary switch and secondary diode voltage stress requirements.

As we know, the Flyback converter is an isolated Buck-Boost type converter. So the AP1682 also can be used in non-isolated Buck-Boost application. The circuit structure and operation principle of Buck-Boost converter with AP1682 is very similar to the Flyback. As shown in Figure 5 and Figure 6, comparing to the Flyback application, the Buck-Boost converter has only inductor instead of transformer, has not primary snubber circuit. The most components of Flyback and Buck-Boost have same design method.

This application notes emphasis on the Flyback power converter design with AP1682. BCD will release the AP1682 design sheet tools for both Flyback and Buck-Boost application to meet the all types of application requirements.

In Buck-Boost application, there is not transformer but an inductor, which means the equivalent turns ratio is 1. In order to match the different design requirements, the K_P, V_S/V_{PK} can be adjusted according to the following equation:

$$K_{LINE} < \frac{\sqrt{2} \cdot V_{in\_rms\_min} \cdot \eta_t}{K_c \cdot \left(V_{o\_max} + V_d + \sqrt{2} \cdot V_{in\_rms\_min} \cdot \eta_t \right)} \tag{15}$$

Therefore, as to the higher output voltage (i.e., >200V_{DC}) Buck-Boost application, the K_P value should be set as the lower so that the converter keep operating at DCM mode. On the other hand, if the output voltage is the lower, the K_P value should be set as the higher, so that the higher diode rectifier conduction duty cycle, the lower primary peak current, and the higher conversion efficiency.

5.2 The Current Sense Resistor Calculation

The primary current sense resistor can be calculated according to equation (13) which is derived from equation (9)

$$R_{cs} = \frac{N_t \cdot V_{CS,EQ} \cdot K_{LINE}^2 \cdot \eta_t}{4 \cdot I_O} = \frac{N_t \cdot K_{LINE}^2 \cdot \eta_t}{9 \cdot I_O} \tag{16}$$

5.3 Transformer Inductance Design

Considering the efficiency and transformer size, the minimum switching frequency at low line input and maximum output loading is set as F_{SW_MIN}, then it can be got

$$V_{o\_max} + V_d = Ls \cdot \frac{I_{pks}}{T_{ons}} = \frac{L_p}{N_t^2} \cdot \frac{N_t \cdot \frac{K_{LINE} \cdot V_{CS\_REF} \cdot \eta_t}{R_{cs}}}{\frac{K_c \cdot K_{LINE}}{F_{sw\_min}}} = \frac{L_p \cdot V_{CS\_REF} \cdot F_{sw\_min} \cdot \eta_t}{N_t \cdot K_c \cdot R_{cs}} \tag{17}$$

From the above equation, the primary inductance L_P is

$$L_p = \frac{N_t \cdot K_c \cdot R_{cs} \cdot (V_{o\_max} + V_d)}{V_{CS\_REF} \cdot F_{sw\_min} \cdot \eta_t} \tag{18}$$

5.4 Transformer Winding Turns Number Design

The worst case operation condition of transformer is at peak voltage area of sine waveform input voltage in the minimum input voltage $V_{IN\_RMS\_MIN}$ and the maximum

output loading. The transformer design should be based on the worst case operation condition.

The effective area of ferrite core is A_e, and the maximum flux density B_m is

$$B_m = \frac{L_p \cdot I_{pk}}{A_e \cdot N_p} = \frac{4 \cdot L_p \cdot I_o}{A_e \cdot N_p \cdot N_t \cdot K_c \cdot K_{LINE} \cdot \eta_t} \quad (19)$$

Then the primary winding turns number N_P is

$$N_p = \frac{4 \cdot L_p \cdot I_o}{A_e \cdot B_m \cdot N_t \cdot K_c \cdot K_{LINE} \cdot \eta_t} \quad (20)$$

Secondary side winding turns number N_S is

$$N_s = \frac{N_p}{N_t} \quad (21)$$

The auxiliary winding turns number N_{aux} is

$$N_{aux} = \frac{N_s \cdot Vcc_{\max}}{V_{o\_\min} + V_d} \quad (22)$$

Here, V_{O_MIN} is the minimum output voltage under the condition of the minimum LED cells and lowest LED cell forward voltage drop, V_{CCmax} is the required maximum VCC voltage at that condition.

5.5 Primary Switch and Secondary Diode Selection

The maximum voltage stress of primary switch is

$$V_{Qds\_\max} = \sqrt{2} \cdot V_{in\_rms\_\max} + N_t * (V_{o\_\max} + V_d) + V_{spk} \quad (23)$$

Here, the V_{SPK} is the spike voltage which is result from the leakage inductance and depends on the primary peak current value and leakage inductance value, approximately about 100V to 200V.

The maximum Drain to Source current (RMS value) is

$$I_{Qd\_RMS\_\max} = \sqrt{\frac{N_t \cdot (V_{o\_\max} + V_d) \cdot K_c \cdot K_{LINE}^2 \cdot V_{CS\_REF}^2}{6\sqrt{2} \cdot R_{cs}^2 \cdot V_{in\_rms\_\min} \cdot \eta_t}} \quad (24)$$

The maximum voltage stress of secondary diode is

$$V_{diode\_\max} = \frac{\sqrt{2} \cdot V_{in\_rms\_\max}}{N_t} + (V_{o\_\max} + V_d) \quad (25)$$

The maximum on status average current of secondary diode is

$$I_{diode\_av\_\max} = \frac{I_{pks}}{2} = \frac{4.5 \cdot I_o}{K_{LINE}} \quad (26)$$

According to the above calculated voltage and current stress, the proper MOSFET and Schottky diode part can be selected as primary switch and secondary rectifier. Certainly, the efficiency and BOM cost are also the important factors for components selection.

5.6 Output Capacitor Selection

From equation (8) it can be seen that the secondary side current includes DC components and double line frequency sine waveform AC component. The AC component of output current is

$$I_{s\_AC} = -\frac{N_t \cdot V_{CS,EQ} \cdot K_{LINE}^2 \cdot \eta_t}{4 \cdot R_{cs}} Cos2\theta = -I_o \cdot Cos2\theta \quad (27)$$

The maximum output ripple current ΔI_O (peak value) is always defined by customer as

$$\Delta I_o = K_{cr} \cdot I_o \quad (28)$$

Generally K_{cr} is less than 30%. As to the definite LED loading, there is a dynamic resistance R_{LED} at DC operation point, which can be calculated with the V-I curve of LED cells. So the output voltage ripple ΔV_O is

$$\Delta V_o = R_{LED} \cdot \Delta I_o \quad (29)$$

The output capacitor is a capacitive load paralleled with output LED, so the output voltage ripple

$$\Delta V_o = R_{LED} \cdot K_{cr} \cdot I_o = I_o \cdot \frac{R_{LED}}{\sqrt{1 + (4 \cdot \pi \cdot F_{line} \cdot C_{out} \cdot R_{LED})^2}} \quad (30)$$

From the above equation, it can be seen that the higher output capacitance, the lower output current ripple. In order to meet output current K_{cr}*I_O requirement, the minimum output capacitance C_{out_min} is

$$C_{out\_\min} > \frac{\sqrt{\frac{1}{K_{cr}^2} - 1}}{4 \cdot \pi \cdot F_{line} \cdot R_{LED}} \quad (31)$$

It can be seen that the higher output current ripple, the higher required output capacitance. The worst case is when K_{cr} is 100%, the required output capacitance is 0, that means the maximum output current ripple amplitude (peak value) equals to the output current average value. The

output ripple current also depends on the output LED loading characteristics. The higher dynamic resistance R_{LED}, the lower output ripple current, the lower required output capacitance.

5.7 Input Voltage Sense Circuit Design

The voltage range of the VS pin and VPK pin is from 0 to clamp level 3.5V. As to most of isolated Flyback application, the K_{LINE}, the maximum value of V_S/V_{PK}, always sets as 1. It is recommended to set the maximum voltage of V_S and V_{PK} as 3V at the maximum input voltage $V_{in\_rms\_max}$. The VS pin resistor divider proportion should be set as

$$\frac{R_6}{R_3+R_4+R_5+R_6}=\frac{3}{\sqrt{2}\cdot V_{in\_rms\_max}} \quad (32)$$

A ceramic capacitor less than 100pF should be placed closely VS pin to GND pin to avoid high frequency noise.

Because VPK pin senses the peak value of sine waveforms, a low pass filter is required to get the average value of sine waveform voltage. So the VPK pin resistor divider proportion should be set as

$$\frac{R_5+R_6}{R_3+R_4+R_5+R_6}=\frac{3\cdot\pi}{2\sqrt{2}\cdot V_{in\_rms\_max}} \quad (33)$$

In order to reduce the power loss on resistor connecting to DC bus, the total resistance of R3+R4+R5+R6 should be as large as possible.

The RC low pass filter consists of R7 and C4. It is recommended use 1μF value for capacitor C4 and 330k for R7 so that the corner frequency should be less than 10Hz.

5.8 FB Pin Sense Circuit Design

Assume VCC auxiliary winding is tightly coupled with primary and secondary winding, the auxiliary winding voltage is

$$V_{AUX}=\frac{N_{AUX}}{N_S}\cdot(V_O+V_d) \quad (34)$$

By sensing FB pin voltage, the LED driver can work at HICCUP mode and keep output voltage below the maximum output voltage limit value under no load or load disconnection conditions. The FB pin voltage at normal operation should be less than the minimum CV threshold, so the voltage divider at FB pin should meet

$$3=\frac{N_{AUX}}{N_S}\cdot(V_O+V_d)\cdot\frac{R_{17}}{R_{16}+R_{17}} \quad (35)$$

5.9 Line Compensation Circuit Design

Because there is a constant delay time T_{d_off} from the time when CS pin voltage reaches the given reference to the time when the real primary peak current reaches peak value, the primary peak current value has a gap ΔI_{pk} with the ideal value

$$\sqrt{2}\cdot V_{in\_rms}\cdot\sin\theta=L_p\cdot\frac{\Delta I_{pk}}{T_{d\_off}} \quad (36)$$

With the different input voltage, the different ΔI_{PK} results in the different constant output current. Therefore, a line compensation circuit is necessary to decrease or eliminate this gap and achieve the better output current accuracy.

A resistor R_{COMP} is connected from DC bus to CS pin in order to cancel the peak current gap ΔI_{pk}. The compensation circuit should meet

$$\sqrt{2}\cdot V_{in\_rms}\cdot\sin\theta\cdot\frac{R_{12}+R_{cs}}{R_{comp}+R_{12}+R_{cs}}=R_{cs}\cdot\Delta I_{pk}$$
$$=\frac{\sqrt{2}\cdot V_{in\_rms}\cdot\sin\theta\cdot T_{d\_off}\cdot R_{cs}}{L_p} \quad (37)$$

Since R_{CS}<<R_{14}, then

$$\frac{R_{12}}{R_{comp}+R_{12}}=\frac{T_{d\_off}\cdot R_{cs}}{L_p} \quad (38)$$

Since the delay time T_{d_off} includes IC internal delay time, about 60ns, and primary switch turn off delay time and fall time, this delay time value should be determined with the real design application.

6. Layout Consideration

The PCB layout rules are highlighted as following:

- The Flyback converter power current flow loop area should be minimized for better EMI performance
- The R-RCD or DZ clamp snubber and output rectifier loop areas should be minimized to achieve good EMI and efficiency performance
- The power ground and signal ground should be connected by one node. Common connection of GND will introduce disturbances to small signals. The ground of transformer must be separate from the ground of IC in order to pass ESD test.
- C6 should be placed as close as possible to Pin VCC of the AP1682 respectively.

7. Design Example

Here is a design example of LED driver to demonstrate the design process of AP1682 solution.

7.1 The Specification

AC mains voltage range: V_{IN}_ac = 85 to 265V_{RMS}

Nominal DC output voltage: V_O=12V
Output constant current: I_O=0.6A
Full load switching frequency: f_{SW}=80kHz
Expected efficiency: η> 80%@120Vac

7.2 The Design Schematic

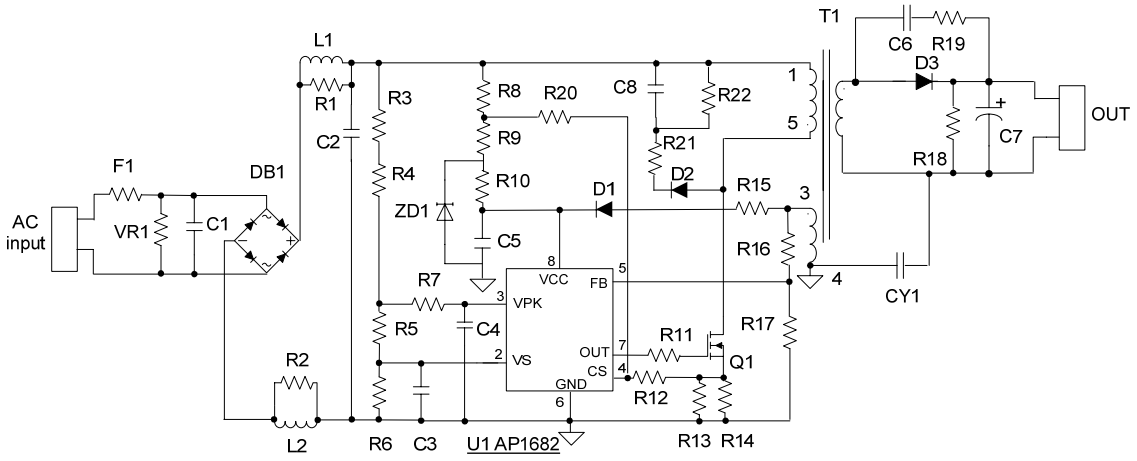

Figure 5. Typical Application Schematic of Isolated Solution with AP1682

7.3 Design Parameter Calculation and Components Selection

7.3.1 Transformer Parameter Determination

For PSR isolated LED driver, the transformer parameters determine the power converter operation status, so firstly transformer design should be frozen, including primary to secondary winding turns ratio, primary winding inductance, etc. It is assumed that the secondary diode forward voltage drop V_d is about 0.4V, transformer converter ratio η_t is about 0.9 and the K_{LINE} value is 1. According to design specification and equation (14), the maximum turn ratio should be

$$N_t < \frac{1.25 \cdot \sqrt{2} \cdot V_{in\_rms\_\min} \cdot \eta_t}{V_o + V_d} = 10.9 \quad (39)$$

Considering the primary switch and secondary diode voltage stress, the N_t is selected as 9.

Then the primary sense resistor R_{CS} is calculated as

$$R_{cs} = \frac{N_t \cdot K_{LINE}^2 \cdot \eta_t}{9 \cdot I_O} = 1.5 \quad (40)$$

The primary winding inductance of transformer L_P is calculated as

$$L_p = \frac{0.444 \cdot N_t \cdot R_{cs} \cdot (V_o + V_d)}{1 \cdot F_{sw\_\min} \cdot \eta_t} = 1.03m \quad (41)$$

Certainly, the calculated results are theoretical value since of some assumed condition and parameter tolerance. So designer need fine-tune these design parameters to match the real design.

According to LED power board size requirements, a EF16 ferrite core is chose as transformer core. The effective area of EF16 is 20.1mm^2, the maximum flux density is set as 0.3T, so the primary winding turns number and secondary winding turn number are

$$N_p = \frac{4 \cdot L_p \cdot I_o}{A_e \cdot B_m \cdot N_t \cdot K_c \cdot K_{LINE} \cdot \eta_t} = 114 \quad (42)$$

$$N_s = \frac{N_p}{N_t} = 12.6 \quad (43)$$

Because transformer winding turns number must be integer, so it can select N_S as 13 T_S, then primary winding turns number should be

$$N_p = N_t \cdot N_s = 117 \quad (44)$$

The VCC_{max} is set as 16V, so the VCC winding turns number is

$$N_{aux} = \frac{N_s \cdot Vcc_{\max}}{V_o + V_d} = 16.7 \approx 17 \quad (45)$$

7.3.2 Power Components Selection

With the designed transformer turns ratio, the primary switch voltage stress is

$$V_{Qds\_max} = \sqrt{2} \cdot V_{in\_rms\_max} + N_t * (V_{o\_max} + V_d) + V_{spk}$$
$$= \sqrt{2} \cdot 265 + 9 \cdot 12.4 + 100 = 586 \quad (46)$$

Here, the V_{SPK} is estimated about 100V. Therefore, a 600V MOSFET device can be used here.

The primary switch maximum RMS current is

$$I_{Qd\_RMS\_max} = \sqrt{\frac{N_t \cdot (V_{o\_max} + V_d) \cdot K_{LINE}^2 \cdot K_c \cdot V_{CS\_REF}^2}{6\sqrt{2} \cdot R_{CS} \cdot V_{in\_rms\_min} \cdot \eta_t}} = 0.226 \quad (47)$$

Actually, in order to achieve the higher efficiency, the much more higher current stress MOSFET is always selected in real design to reduce the conduction power loss.

The secondary diode voltage stress is

$$V_{diode\_max} = \frac{\sqrt{2} \cdot V_{in\_rms\_max}}{N_t} + (V_{o\_max} + V_d) = 54 \quad (48)$$

The maximum on status average current is

$$I_{diode\_av\_max} = \frac{4.5 \cdot I_o}{K_{LINE}} = 2.7 \quad (49)$$

A 60V/3A Schottky diode SB360 can be selected here. If the higher efficiency is required, the higher current rating diode is preferred.

7.3.3 Output Capacitance Calculation

A big capacitance output capacitor is needed to eliminate the double line frequency output current ripple. This ripple is also relative to LED loading characteristics, dynamic resistance R_{LED} near DC value current.

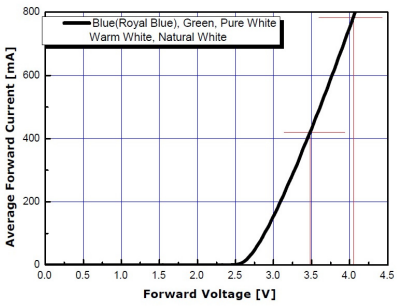

Figure 6. LED Cell Forward V-I Curve

Figure 6 shows the LED cell in design example forward voltage forward current V-I curve characteristics. At the output current DC operation point, the current variation of each LED cell is 0.42A to 0.78A, and voltage variation is 3.45V to 4.1V. The output loading uses 4 pieces LED cells in series. So the dynamic resistance R_{LED} is

$$R_{LED} = \frac{4 \cdot \Delta V_{LED}}{\Delta I_{LED}} = \frac{4 \cdot (4.1 - 3.45)}{0.78 - 0.42} = 7.22 \quad (50)$$

The required output current ripple is defined as 30% of output current, K_{cr}=0.3. So at the 50Hz AC frequency condition, the required output capacitance should be

$$C_{out\_min} > \frac{\sqrt{\frac{1}{K_{cr}^2} - 1}}{4 \cdot \pi \cdot F_{line} \cdot R_{LED}} = 700\mu F \quad (51)$$

7.3.4 External Circuit Design of AP1682

The maximum value of VPK pin is set as 3V, so the proportion of VPK sense circuit is as

$$\frac{R_5 + R_6}{R_3 + R_4 + R_5 + R_6} = \frac{3 \cdot \pi}{2\sqrt{2} \cdot V_{in\_rms\_max}} = \frac{3 \cdot \pi}{2\sqrt{2} \cdot 265} \quad (52)$$

If R3 and R4 is selected as 1M, so the R5+R6 is calculated as about 25.4k. In order to achieve the DC average value of half rectified sine waveform, the low pass filter is necessary. So a 0.33µF capacitor C4 is paralleled with R7 of 330K here.

The maximum value of VS pin is also set as 3V, so the proportion of VS sense circuit is as

$$\frac{R_6}{R_3 + R_4 + R_5 + R_6} = \frac{3}{\sqrt{2} \cdot V_{in\_rms\_max}} = \frac{3}{\sqrt{2} \cdot 265} \quad (53)$$

So the R6 is calculated as about 16.2K. A ceramic capacitor C3 is paralleled between VS pin and Ground to bypass the high frequency noise. Too high capacitance will result in the distortion of sine waveform current reference, and then the worse Power Factor. So the capacitor less than 100pF value is recommended.

The FB pin resistor divider is used to detect output voltage so that the power board can operate at no load condition. The FB pin OVP threshold is 4V, therefore, the resistor divider proportion is

$$\frac{R_{17}}{R_{16} + R_{17}} = \frac{3 \cdot N_S}{N_{AUX} \cdot (V_O + V_d)} \quad (54)$$

Here, R16=52.3k and R17=12k are selected.

The line compensation resistor value meet equation (55), if the T_{d_off} is assumed about 80ns, so the line compensation resistor is

$$R_{line}=\frac{R_{14}\cdot\left(1-\frac{T_{d\_off}\cdot R_{cs}}{L_p}\right)}{\frac{T_{d\_off}\cdot R_{cs}}{L_p}}=\frac{2.4K\cdot\left(1-\frac{80n\cdot 1.5}{1m}\right)}{\frac{80n\cdot 1.5}{1m}}\approx 20M \quad (55)$$

In order to reduce the components quantity, a resistor R20 is connected to the point between 2 start-up resistors R8=R9=750K. Since the R8 and R9 value is much less than line compensation resistor value, the R20 is about half of line compensation value, 10M.

7.4 The Material BOM List of Isolated Solution with AP1682

Item	Description	QTY
C1	33nF/400V, X-capacitor	1
C2	100nF/400V, capacitor CL21	1
C3	100pF/16V, 0603, ceramic capacitor	1
C4	330nF/16V, 0603, ceramic capacitor	1
C5	1μF/25V, 1206, ceramic capacitor	1
C6	1nF/100V, 1206, ceramic capacitor	1
C7	1500μF/16V, 105ºC, 10mm*20mm electrolytic capacitor	1
C8	1nF/ 500V 0805, ceramic capacitor	1
CY1	2.2nF/275V, Y safety capacitor	1
D1	Diode, 1N4148, SOD-323	1
D2	1A/600V, SMA, US1J	1
D3	BCD, APD360VRT-G1, 3A/60V, Schottky diode, SMA	1
ZD1	TVS 150V, SMA	1
L1,L2	7.5mH, Inductor,Φ6.5mm*12.5mm	2
F1	Fuse, 1.25A/250V	1
VR1	Varistor 07D471K	1
BD1	0.5A/600V,TO-269AA,MB6S	1
R1,R2	10KΩ, 5%, 1206, resistor	2
R3, R4	1MΩ, 1%,1206, resistor	2
R5	11KΩ, 1%, 0603, resistor	1
R6	16KΩ, 1%,0603, resistor	1
R7	330KΩ, 5%,0603, resistor	1

Item	Description	QTY
R8,R9	750KΩ, 5%,1206, resistor	2
R10	100KΩ, 5%,0603, resistor	1
R11	20Ω, 5%,0603 , resistor	1
R12	3K3, 5%,0603 , resistor	1
R13	2R4, 1%,1206 , resistor	1
R14	3R3, 1%, 1206, resistor	1
R15	10Ω, 5%, 0805, resistor	1
R16	52.3KΩ, 1%,0603 , resistor	1
R17	12KΩ, 1%,0603 , resistor	1
R18	18KΩ, 5%,1206, resistor	1
R19	100Ω, 5%,1206, resistor	1
R20	10MΩ, 5%, 1206, resistor	1
R21	47R, 5%, 1206, resistor	1
R22	200KΩ, 5%, 1206, resistor	1
T1	EF16 10 pin 950μH, 5%,Transformer	1
U1	AP1682MTR-G1, SOIC-8, BCD's IC	1
Q1	MOSFET, Infineon, SPI04N60, 4A/600V ,TO-251	1

7.5 Transformer Specifications

7.5.1. Electrical Diagram

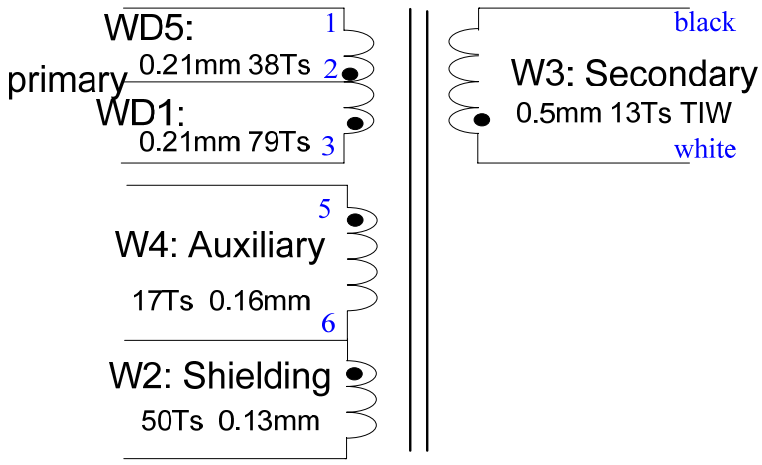

Figure 7. Transformer Electrical Schematic Diagram

7.5.2. Electrical Specifications

Primary Inductance	Pin 1-3, all other windings open, measured at 1kHz, 0.4V_{RMS}	1000μH, ±5%
Primary Leakage Inductance	Pin1-3, all other windings shorted, measured at 10kHz, 0.4V_{RMS}	50μH (Max)
Electrical Strength	60 seconds, 60Hz, from Pin 1-5 to Pin 6-10	3000Vac

7.5.3. Materials

Item	Description
1	Core: EF16, PC40 or equivalent
2	Bobbin: EF16, Horizontal, 12 Pin, (6/6)
3	Wire:ø0.13mm, for internal wire shielding winding
4	Wire: ø0.21mm, for the Primary winding
5	Wire: ø0.16mm, for the Auxiliary winding
6	Triple Insulated Wire: ø0.5mm for Secondary Winding
7	Tape: 0.05mm thick, 10mm wide
8	Glue: DELO AD895

7.5.4 Transformer Winding Construction Diagram

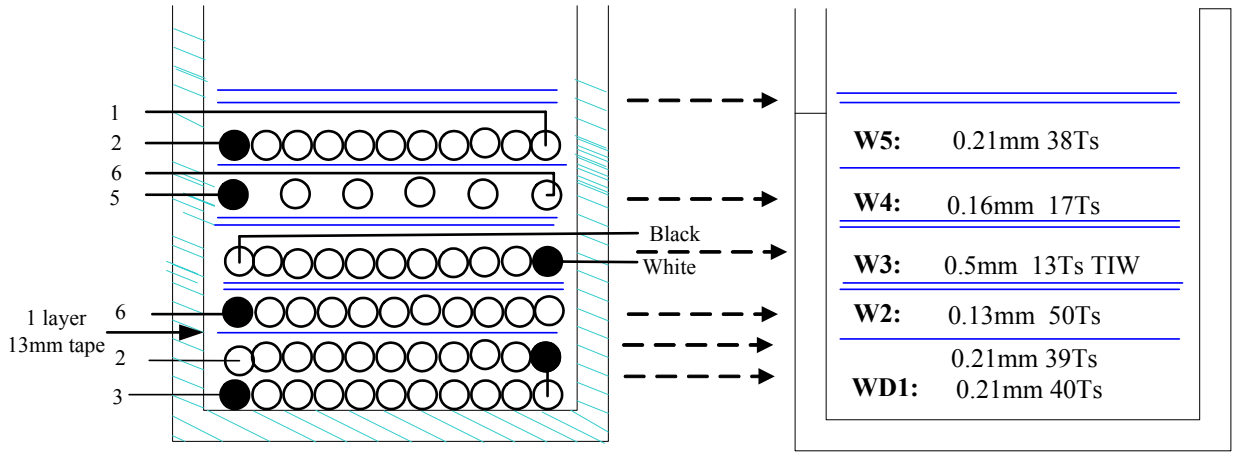

Figure 8. Transformer Winding Construction Diagram

Winding Sequence: Begin from the central column of the Bobbin. Primary side of the bobbin is placed on the left hand side, and secondary side of the bobbin is placed on the right hand side.	
W1 Primary winding	Start at Pin 3. Wind 40 turns of ø0.21 mm wire [4] from left to right. Wind another 39 turns on the next layer from right to left. Finish on Pin 2. Wind tightly & spread evenly.
Insulation	1 Layer of insulation tape [7], 0.05mm thick, 10.0mm wide.
W2 Shielding winding	Start at Pin 6. Wind 62 turns of ø0.16mm wire [3] from left to right. The terminal floats. Wind tightly & spread evenly.
Insulation	2 Layers of insulation tape [7], 0.05mm thick, 10.0mm wide.
W3 Secondary Winding	Start at white terminal. Wind 13 turns of ø0.5mm Triple Insulated Wire [6] from left to right. Finish with black terminal. Wind tightly & spread evenly.
Insulation	2 Layers of insulation tape [7], 0.05mm thick, 10.0mm wide.
W4 Auxiliary winding	Start at Pin 5. Wind 17 turns of ø0.16mm wire [5] from left to right. Finish on Pin 6. Wind tightly & spread evenly.
Insulation	1 Layer of insulation tape [7], 0.05mm thick, 10.0mm wide.
W5 Primary winding	Start at Pin 2. Wind 38 turns of ø0.21mm wire [4] from left to right, Finish on Pin 1. Wind tightly & spread evenly.
Insulation	2 Layers of insulation tape [8], 0.05mm thick, 10.0mm wide.
Glue	Glue[8] core and bobbin
	Core short to Pin5

7.6 PCB Layout

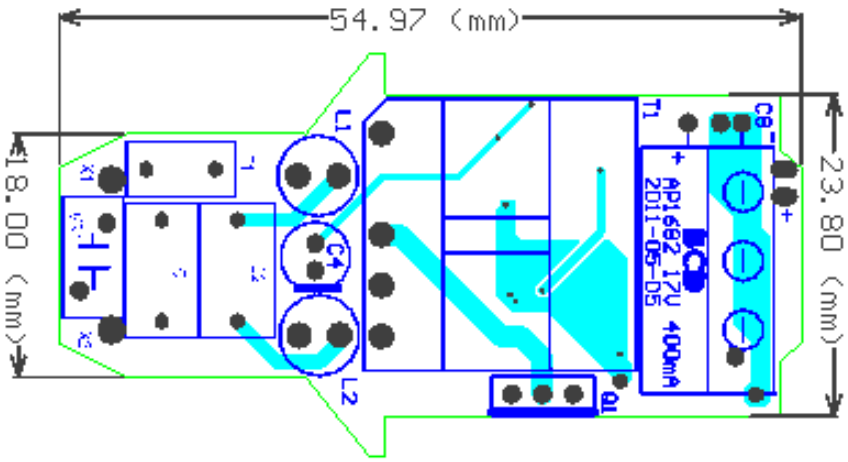

Figure 9. Demo Board PCB and Component Layout (Top View)

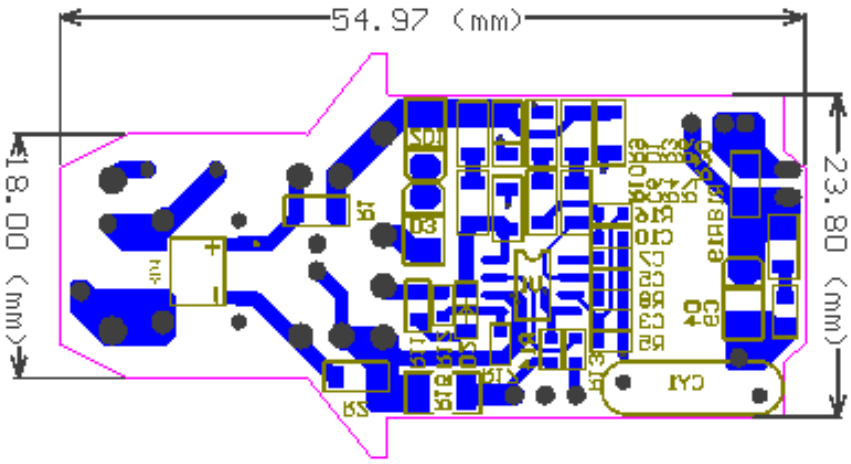

Figure 10. Demo Board PCB and Component Layout (Bottom View)

7.7 Test Result

7.7.1 Full Load Efficiency

Input Condition	P_{IN} (W)	V_O (V_{DC})	I_O (A_{DC})	P_O (W)	Efficiency
120V_{AC}/60Hz	9.79	12.58	0.614	7.91	80.8%
230V_{AC}/50Hz	9.63	12.58	0.614	7.93	82.3%

7.7.2 Output Current Regulation

Input Voltage (V_{AC})	Output Current (A)			Load Regulation (%)
	3 LEDs	4 LEDs	5 LEDs	
85	0.622	0.610	0.594	**2.30%**
100	0.623	0.612	0.595	**2.30%**
110	0.623	0.613	0.596	**2.21%**
120	0.623	0.613	0.596	**2.21%**
130	0.623	0.613	0.596	**2.21%**
150	0.622	0.613	0.597	**2.05%**
170	0.621	0.614	0.597	**1.97%**
190	0.620	0.614	0.599	**1.72%**
220	0.620	0.614	0.600	**1.64%**
230	0.619	0.614	0.600	**1.56%**
240	0.618	0.614	0.601	**1.39%**
265	0.615	0.612	0.601	**1.15%**
Line Regulation (%)	**0.65%**	**0.33%**	**0.59%**	**2.38%**

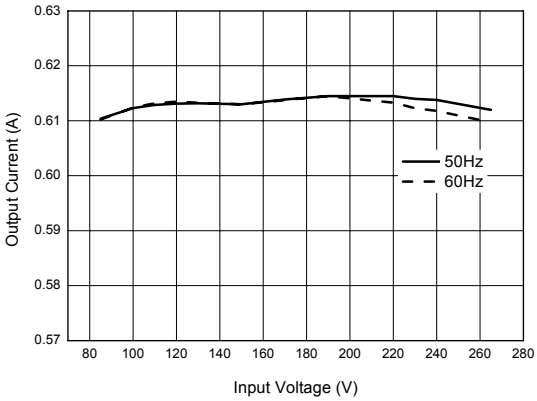

Figure 11. Line Regulation of Output Current at Full Load

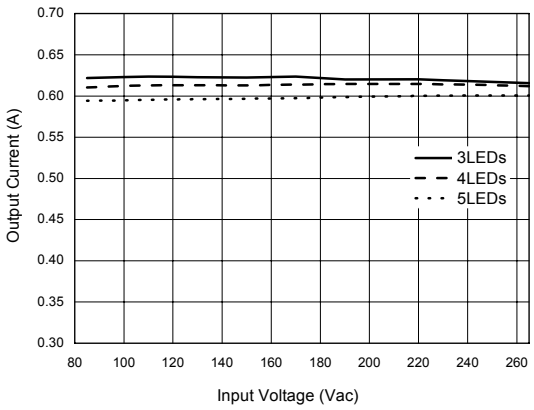

Figure 12. Load Regulation of Output Current

7.7.3 Power Factor and Harmonics

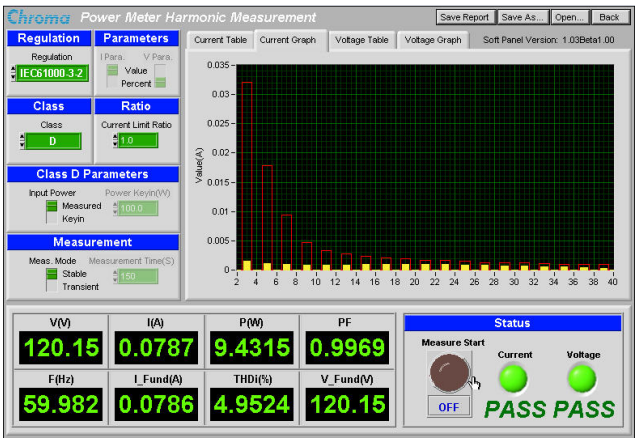

Figure 13. Full Load Power Factor & THD @ 120Vac

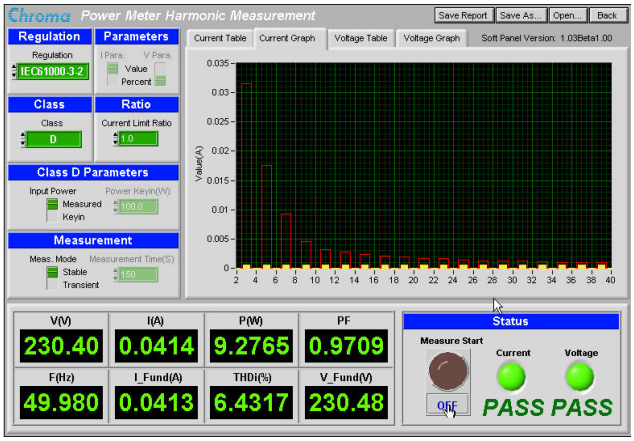

Figure 14. Full Load Power Factor & THD @ 230Vac

8. Non-isolated Buck-Boost Design Example

Here is another non-isolated Buck-Boost design example of LED driver with AP1682 solution. The design specification is

8.1 The Specification

AC mains voltage range: V_{IN}_ac = 85 to 265V_{RMS}

Nominal DC output voltage: V_O=100V
Output constant current: I_O=93mA
Expected efficiency: η> 90%

8.2 The Non-isolated Buck-Boost Design Schematic

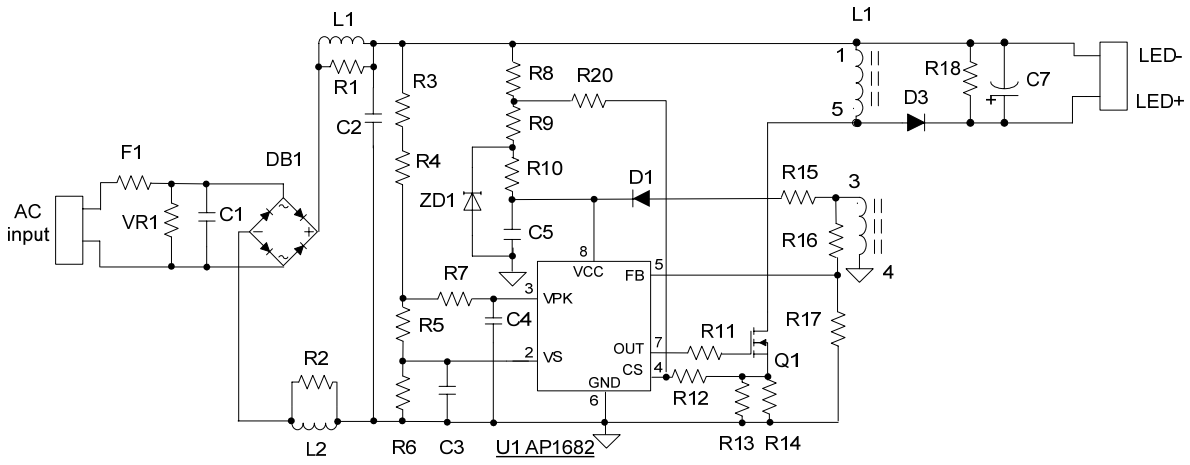

Figure 15. Typical Application Schematic of Non-isolated Solution with AP1682

8.3 The Material BOM List of Non-isolated Solution with AP1682

Item	Description	QTY
C1	33nF/400V, X-capacitor	1
C2	100nF/400V, capacitor CL21	1
C3	100pF/16V, 0603, ceramic capacitor	1
C4	330nF/16V, 0603, ceramic capacitor	1
C5	1μF/25V, 1206, ceramic capacitor	1
C7	33μF/160V, 105°C, 10mm*20mm electrolytic capacitor	1
D1	Diode, 1N4148, SOD-323	1
D3	ES1J, 1A/600V, SMA	1
L1,L2	4.7mH, Inductor,Φ8mm*12.5mm	2
F1	Fuse, 1.25A/250V	1
VR1	Varistor 07D471K	1
BD1	0.5A/600V,TO-269AA,MB6S	1
R1,R2	10KΩ, 5%, 1206, resistor	2
R3, R4	750KΩ, 1%,1206, resistor	2
R5	4K7Ω, 1%, 0603, resistor	1
R6	12KΩ, 1%,0603, resistor	1
R7	330KΩ, 5%,0603, resistor	1

Item	Description	QTY
R8, R9	750KΩ, 5%,1206, resistor	2
R10	100KΩ, 5%,0603, resistor	1
R11	20Ω, 5%,0603 , resistor	1
R12	3KΩ, 5%,0603 , resistor	1
R13	1R5, 1%,1206 , resistor	1
R14	1R6, 1%, 1206, resistor	1
R15	10Ω, 5%, 0805, resistor	1
R16	56KΩ, 1%,0603 , resistor	1
R17	12KΩ, 1%,0603 , resistor	1
R18	680KΩ, 5%,1206, resistor	1
R20	8M2, 5%, 1206, resistor	1
T1	EE16-7.2 6 pin 1.3mH, 5%,Transformer	1
U1	AP1682MTR-G1, SOIC-8, BCD's IC	1
Q1	MOSFET, Infineon, SPI04N60, 4A/600V ,TO-251	1